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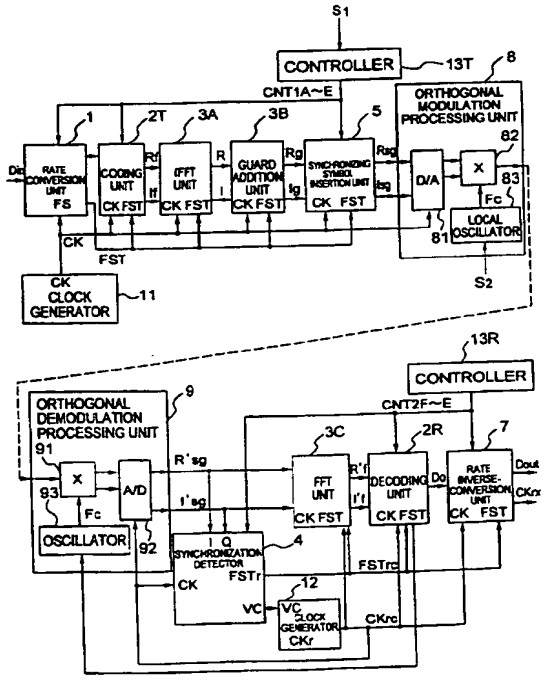
(54) Multicarrier transmission system, with modifiable bandwidth

(57) A communication method in an orthogonal frequency division multiplexing modulation communication system includes a transmission apparatus (1, 2T, 3A, 3B, 5, 8, 11, 13T) in which a frequency bandwidth of a signal modulated in accordance with an orthogonal frequency division multiplexing modulation system is changed and the modulated signal is transmitted and a receiving apparatus (9, 4, 12, 3C, 2R, 7, 13R) in which the modulated signal is received and a frequency bandwidth for demodulation of the received signal is changed to follow the change of the frequency bandwidth of the modulated signal.

FIG. 1



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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a transmission bandwidth changing method and a digital transmission apparatus for an orthogonal frequency division multiplexing modulation system.

[0002] In recent years, in Europe, the United States of America and Japan, the digitalization of the television broadcasting is being studied, while the orthogonal frequency division multiplexing (OFDM) modulation system is promising as the modulation system of the digitalization.

[0003] The OFDM modulation system is of a kind of multi-carrier modulation system and a multiplicity of digital modulation waves are added to one another to be transmitted. The quadrature phase shift keying (QPSK) system, the quadrature amplitude modulation system or the like is used as the modulation system of carriers thereof.

[0004] An OFDM signal is expressed by equations as follows:

[0005] First, when a QPSK signal of each carrier is $\alpha_k(t)$, the signal is expressed by the following equation (1):

$$\alpha_k(t) = a_k(t)\times\cos(2\pi kft)+b_k(t)\times\sin(2\pi kft) \quad (1)$$

where k represents a number of the carrier, and $a_k(t)$ and $b_k(t)$ represent data of the k-th carrier and have a value of [-1] or [1].

[0006] Next, when the number of carriers are N, the OFDM signal is a composite signal of N carriers and when the composite signal is $\beta_k(t)$, the signal can be expressed by the following equation (2):

$$\beta_k(t) = \Sigma\alpha_k(t) \quad (2)$$

where k assumes 1 to N, that is, k=1 to N (which is an integer equal to or larger than 1).

[0007] The OFDM signal is constituted by a time-axis base signal defined by the equation (2). For example, 32 samples of guard interval data are added to 1024 effective samples of data to constitute one symbol of 1056 samples and 396 sets of symbols are added to 4 sets of synchronizing symbols to constitute a series of signals of 400 symbols in total. The series of signals of 400 symbols is named a frame. The OFDM signal is constituted by frames generated repeatedly.

[0008] The digital communication technique using the OFDM system is described in, for example, a paper on "A Study on Field Pickup Unit using OFDM Modulation Scheme", Shigeki Moriyama et al., ITE Technical Report Vol. 19, No. 38, pp. 7-17, Aug. 1955 and JP-A-7-30513. In the conventional OFDM system, a frequency bandwidth of a signal to be transmitted is a fixed value previously assigned to a communication system and is not changed.

SUMMARY OF THE INVENTION

[0009] According to the present invention, there is provided an OFDM system having a changeable frequency bandwidth for a transmission signal. When the bandwidth is changed in the transmission side, a demodulation bandwidth for a received signal is changed to follow the changed bandwidth of the transmission signal in a receiving side. The transmission frequency bandwidth in the OFDM system is expressed by a product of an interval of frequency between adjacent carriers and the number of total carriers. According to an embodiment of the present invention, the frequency bandwidth is changed by changing the number of carriers or by changing the interval between carriers.

[0010] In the digital communication system utilizing the present invention, the frequency bandwidth assigned for transmission of a digital signal can be employed effectively. The bandwidth can be broadened in the communication requiring a wide bandwidth as an image signal and the bandwidth can be narrowed in the transmission of a signal having a relatively narrow bandwidth as an audio signal and a control signal. Further, when the occupancy frequency bandwidth required for a signal to be transmitted is narrower than the assigned frequency bandwidth, the assigned bandwidth is divided into a plurality of channels each having a narrower bandwidth, so that different data can be transmitted by means of the plurality of channels. Bidirectional communication can be attained by means of the plurality of channels. In addition, occupied bandwidth of each channel can be changed or shifted in accordance with the amount of transmitted data on the way to thereby change the quality of the transmission signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]

Fig. 1 is a block diagram schematically illustrating the overall configuration of an OFDM communication system

according to an embodiment of the present invention;

Fig. 2 is a block diagram schematically illustrating the overall configuration of an OFDM communication system according to another embodiment of the present invention;

Fig. 3 is a block diagram schematically illustrating the overall configuration of an OFDM communication system according to still another embodiment of the present invention;

Fig. 4 is a block diagram schematically illustrating the overall configuration of an embodiment of an automatic bandwidth changeable transmission system to which the present invention is applied;

Fig. 5 is a timing chart showing operation of the embodiment of the present invention in case where the number of carriers is changed;

Fig. 6 shows states of frequency components in the embodiment of the present invention in case where the number of carriers is changed;

Fig. 7 is a timing chart showing operation of the embodiment of the present invention in case where the number of symbols is changed;

Fig. 8 is a block diagram schematically illustrating a rate conversion unit 1 used in the system according to the embodiment of the present invention;

Fig. 9 is a block diagram schematically illustrating a coding unit 2T used in the system according to the embodiment of the present invention;

Fig. 10 is a block diagram schematically illustrating a synchronizing symbol insertion unit 5 used in the system according to the embodiment of the present invention;

Fig. 11 is a block diagram schematically illustrating synchronization detection units 4 and 15 used in the system according to the embodiment of the present invention;

Fig. 12 is a block diagram schematically illustrating a decoding unit 2R used in the system according to the embodiment of the present invention;

Fig. 13 is a block diagram schematically illustrating a rate inverse-conversion unit 7 used in the system according to the embodiment of the present invention;

Fig. 14 is a block diagram schematically illustrating the overall configuration of the OFDM communication system to which the system of the present invention can be applied;

Figs. 15A and 15B are a timing chart showing waveforms at various portions of the OFDM communication system and a waveform diagram showing a frame structure, respectively;

Fig. 16 is a block diagram schematically illustrating a rate conversion unit used in the communication system illustrated in Fig. 14;

Fig. 17 is a block diagram schematically illustrating a coding unit used in the communication system illustrated in Fig. 14;

Fig. 18 is a block diagram schematically illustrating an IFFT unit used in the communication system illustrated in Fig. 14;

Fig. 19 is a block diagram schematically illustrating a guard addition unit used in the communication system illustrated in Fig. 14;

Fig. 20 is a block diagram schematically illustrating a synchronizing symbol insertion unit used in the communication system illustrated in Fig. 14;

Fig. 21 is a block diagram schematically illustrating a synchronization detection unit used in the communication system illustrated in Fig. 14;

Fig. 22 is a diagram showing operation of an IFFT transform unit used in the communication system illustrated in Fig. 14;

Figs. 23A and 23B are timing charts of signals for explaining operation of a data confirmation unit in the embodiment of the present invention;

Fig. 23C is a block diagram schematically illustrating the data confirmation unit;

Fig. 24 is a block diagram schematically illustrating an example of a circuit state monitoring unit in the embodiment of the present invention;

Fig. 25 is a block diagram schematically illustrating the overall configuration of an OFDM communication system according to a further embodiment of the present invention;

Figs. 26A and 26B are diagrams for explaining a relation of an interval between carriers and a frequency bandwidth;

Fig. 27 is a block diagram schematically illustrating a synchronization detection unit 15 used in the system according to the embodiment of the present invention;

Fig. 28 is a block diagram schematically illustrating the overall configuration of an OFDM communication system according to a still further embodiment of the present invention;

Fig. 29 is a block diagram schematically illustrating the overall configuration of an OFDM communication system according to a still further embodiment of the present invention;

Fig. 30 is a block diagram schematically illustrating the overall configuration of an embodiment of an automatic bandwidth changeable transmission system to which the present invention is applied;

Fig. 31 shows a relation of a frame period time and frequency component in case where the clock rate is equal to one time of the original frequency; and

Fig. 32 shows a relation of the frame period time and the frequency component in an increased clock rate.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0012] Embodiments of the present invention are now described in detail with reference to the accompanying drawings.

[0013] Fig. 14 is a block diagram schematically illustrating a digital communication system using the OFDM modulation system to which the technique of the present invention can be applied, and Figs. 15A and 15B are timing charts of signals at various portions of the system.

[0014] Data Din successively inputted are rate-converted by a rate conversion unit 21, which produces data Dii during the period excluding a four-symbol period corresponding to a synchronizing symbol period described later and the period excluding blanks for unnecessary carriers corresponding to the period of 344-th to 679-th samples in each information symbol at intervals of a frame period composed of 400 symbols.

[0015] Further, the rate conversion unit 21 supplies an FST signal indicating the beginning of the synchronizing symbol period to other units every 400 symbols corresponding to the frame period.

[0016] A coding unit 22T codes the input data to produce coded data Rf and If mapped in two axes of I and Q.

[0017] An IFFT (Inverse Fast Fourier Transform) unit 3A regards the coded data Rf and If as frequency components and converts the data into time-axis signals R and I including 1024 samples.

[0018] A guard addition unit 3B adds waveforms at the beginning period of the signals R and I including 1024 samples, for example waveforms of the first 32 samples, to the end of the 1024 samples and produces time waveform signals Rg and Ig of 1056 samples in total.

[0019] A synchronizing symbol insertion unit 25 prepares signals Rsg and Isg having the synchronizing symbols inserted therein and which are stored previously in a memory and constituted by, for example, 4 symbols and outputs the signals Rsg and Isg at intervals of m information symbols.

[0020] The signals are orthogonally modulated by an orthogonal modulation processing unit 8 to be an OFDM modulation wave signal having a frame structure as shown in Fig. 15B and the OFDM modulation wave signal is transmitted from the transmission side to the reception side.

[0021] A clock CK generated by a clock oscillator 11 is supplied to each of the units.

[0022] The transmitted OFDM modulation wave signal is orthogonally demodulated to an OFDM signal of baseband by an orthogonal demodulation processing unit 9 at the reception side to be outputted as time-axis signals R'sg and I'sg.

[0023] The signals R'sg and I'sg are supplied to a synchronization detector 15, which detects the synchronizing symbol group and produces an FST'r pulse indicating the frame period to be supplied to each unit.

[0024] Further, the time-axis signals R'sg and I'sg are supplied to an FFT unit 3C to be converted from the time waveform signals into frequency component signals R'f and I'f.

[0025] The signals R'f and I'f are decoded by a decoding unit 22R, which produces a signal D'o. The signal D'o is converted into a successive data signal Dout by a rate inverse-conversion unit 27 to be outputted.

[0026] Detailed configuration and operation of each unit are now described.

[0027] First of all, an example of the rate conversion unit 21 is described with reference to Fig. 16.

[0028] The clock CK supplied to the rate conversion unit 21 is inputted to a PLL/VCO 21-2, which produces a clock CKm having a frequency equal to N/G times of the clock CK. The symbol G is a control constant. The relation of the output clock frequency CK of the clock generator 11, the clock frequency CKm in the rate conversion unit 21 and the constant G is expressed by the following equation (3):

$$CKm = CK.\ G = CK.\ N.\ (\text{number of data symbols}).\ (\text{number of modulation bits})/(\text{number of effective samples} + \text{number of guard samples}).\ (\text{number of frame symbols}) \quad (3)$$

[0029] Further, the clock CK is also inputted to an FST counter 21-4, which produces an FST pulse which is a frame reference for processing at the transmission side. The FST pulse is supplied to a WRST terminal and an RRST terminal of an FIFO memory 21-3 to function as a reference for reset in writing and reading operations.

[0030] Reading-out of data from the FIFO memory 21-3 is performed in accordance with a level at an RE terminal in

synchronism with the clock supplied to an RCK terminal thereof. A pulse supplied to the RE terminal is outputted from a decoder 21-5.

[0031] The successively inputted data Din is converted into a parallel signal by a serial-to-parallel (S/P) converter 21-1 to be inputted to the FIFO memory 21-3, which produces the data signal Dii (Fig. 15A) having the blank periods as described above.

[0032] An example of the coding unit 22T is now described with reference to Fig. 17.

[0033] The output signal Dii produced by the rate conversion unit 21 is supplied to mapping ROMs 22-1 and 22-2 to be converted into signals at predetermined points of I and Q axes. The signals during the periods corresponding to the unnecessary carriers shown in Fig. 15A are substituted with "0" in selectors 22-3 and 22-4, so that the signals Rf and If are produced. The selectors 22-3 and 22-4 are controlled by a controller 22-5 having the timing defined on the basis of the clock CK and the FST pulse.

[0034] An example of the IFFT transform unit 3A is now described with reference to Fig. 18.

[0035] The input signals Rf and If are converted into the time waveform signals R and I on the basis of the signal having the symbol period including the guard period by a controller 3A-2 having the timing determined by the clock CK and the FST pulse. The IFFT transform unit can be realized by using PDSP 16510 of Plessy Company, for example.

[0036] An example of the guard addition unit 3B is now described with reference to Fig. 19.

[0037] The input signals R and I are supplied to delay units 3B-1 and 3B-2 for delaying signals by 1024 samples and selectors 3B-3 and 3B-4. The selectors 3B-3 and 3B-4 select undelayed signals R and I for 1st to 1024th samples and signals delayed by 1024 samples in the delay units 3B-1 and 3B-2 for 1025th to 1056th samples to be produced.

[0038] Consequently, the output signals Rg and Ig having 1056 samples for one symbol include the 1025th to 1056th samples to which time waveforms from 1 to 32 samples are added. The selectors 3B-3 and 3B-4 are controlled by a controller 3B-5 having the timing determined by the clock CK and the FST pulse.

[0039] An example of the synchronizing symbol insertion unit 25 is now described with reference to Fig. 20.

[0040] ROMs 25-1 and 25-2 controlled by a controller 25-5 having the timing determined by the clock CK and the FST pulse produce the synchronizing symbol signals at the timing according to the FST pulse.

[0041] Similarly, selectors 25-3 and 25-4 controlled by a controller having the timing determined by the clock CK and the FST pulse select the synchronizing symbol signals from the ROMs 25-1 and 25-2 only during four symbol periods, which are no-signal periods at the current stage, of the guard-added time signals Rg and Ig produced by the guard addition unit 3B. Consequently, the synchronizing symbol insertion unit 25 produces the time waveform signals Rsg and Isg having the synchronizing symbol signal inserted therein as shown in Fig. 15A.

[0042] A NULL symbol shown in Fig. 15B is used to find the presence of the synchronizing symbol group roughly and any signal is not produced during this symbol period.

[0043] Further, a SWEEP symbol is to detect a change point of each symbol exactly and is constituted by a waveform having the frequency varying from a lower limit frequency to an upper limit frequency of the transmission bandwidth during one symbol period.

[0044] A real number part signal Rsg and an imaginary number part signal Isg of the time waveform signals are converted into analog signals in a D/A converter 81 of the orthogonal modulation processing unit 8 and an orthogonal modulator 82 orthogonally modulates the analog signals for the real number part signal with a carrier signal having a frequency fc produced by a local oscillator 83 and the analog signals for the imaginary number part signal with a 90° phase-shifted signal of the carrier signal having the frequency fc produced by the local oscillator 83 and combines both the signals to produce the OFDM signal.

[0045] Configuration and operation of the receiving side are now described.

[0046] First, the signal transmitted as described above and having the frame structure is inputted to the orthogonal demodulation processing unit 9. The unit 9 orthogonally demodulates the input signal with a carrier signal from a voltage-controlled oscillator 93 to take out the real number part signal and orthogonally demodulates the input signal with the 90° phase-shifted carrier signal to take out the imaginary number part signal. The demodulated analog signals for the real number part signal and the imaginary number part signal are converted into digital signals in an A/D converter 92.

[0047] An example of the synchronization detector 15 is now described with reference to Fig. 21.

[0048] The orthogonally demodulated digital signals R'sg and I'sg are inputted to an end-of-NULL detector 15-1 and a SWEEP calculation unit 15-2.

[0049] The end-of-NULL detector 15-1 detects the NULL symbol having the no-signal period from the symbol group having the frame structure to detect a rough position of the synchronizing symbol, so that the detector 15-1 presumes the beginning time of the SWEEP symbol by a timer circuit not shown on the basis of the NULL completion time to produce a SWEEP period flag pulse.

[0050] The SWEEP calculation unit 15-2 searches for an exact change timing of each symbol in accordance with the SWEEP symbol subsequent to the NULL symbol with reference to the SWEEP period flag pulse. More particularly, a pattern of the SWEEP symbol is previously stored in a memory 15-3 and the inputted OFDM signal are correlated with

the signal stored in the memory, so that when the signal pattern stored in the memory and the pattern of the inputted OFDM signal are coincident, a coincidence pulse is inputted to a reset terminal of a frame counter 15-4.

[0051] When a count of the frame counter 15-4 reaches a value constituting the frame period, for example, 422400 (=1056×400), the frame counter resets the count to zero and produces an FSTr pulse indicating the beginning time of the frame. At the same time, the frame counter starts the counting again.

[0052] Thereafter, the frame counter produces the FSTr pulse at intervals of a predetermined count, that is, every beginning point of the frame to thereby indicate the beginning time of the frame. In the receiving side, the FSTr pulse is used as the start timing in the FFT unit 3C, the decoding unit 22R and the rate inverse-conversion unit 27.

[0053] The FFC unit 3C partitions the symbols on the basis of the FSTr pulse and performs the Fourier Transform to thereby attain the OFDM demodulation so that the FFC unit 3C produces the frequency component signals R'f and I'f. The decoding unit 22R identifies the signals R'f and I'f by means of an ROM table method, for example, to calculate the decoded signal D'o.

[0054] The rate inverse-conversion unit 27 determines the operation timing in accordance with the clock CKr and FSTr pulses and has the configuration obtained by inverting the configuration of the rate conversion unit 21.

[0055] The bandwidth of the OFDM signal to be transmitted is twice the bandwidth of the baseband signals Rsg and Isg. The bandwidth of the baseband signals Rsg and Isg is determined depending on data corresponding to the carrier inputted to the IFFT unit 3A.

[0056] Operation of the IFFT unit 3A is now described with reference to Fig. 22. The signal Rf of the frequency component is successively inputted in synchronism with the clock of a period 1/S.

[0057] A first data fo determines an amplitude level of a carrier 0 which is a DC component. A second data f1 determines an amplitude level of a carrier 1 of a period 1024/S. A third data f2 determines an amplitude level of a carrier 2 of a period 512/S.

[0058] A maximum frequency component thus inputted determines a maximum frequency of the time waveforms, that is, the bandwidth prepared by the IFFT transform.

[0059] The carriers prepared by subjecting individually determined amplitudes to the transform are all added to prepare the time waveform signal R.

[0060] The time waveform signal R is constituted by data of 1024 samples in total and each sample data is produced in synchronism with the clock of the period 1/S. That is, the frequency of the carrier 1 is 1024 times the input clock frequency.

[0061] The carrier interval is determined by the number of FFT samples and the FFT clock.

$$\text{Carrier Interval} = \text{Number of FFT Samples} \times 1/(\text{FFT Clock Frequency})$$

[0062] Further, the bandwidth is determined by the carrier interval and the number of carriers.

$$\text{Bandwidth} = \text{Carrier Interval} \times \text{Number of Carriers} \quad (4)$$

[0063] The digital communication system of the OFDM modulation system described with reference to the accompanying drawings can utilize the system and the method disclosed in co-pending U.S. Patent Application Serial No. 09/098,346 filed on June 17, 1998 and Serial No. 09/099,390 filed on June 18, 1988 filed by inventors including the inventor of the present invention. The disclosure of these co-pending applications are incorporated herein by reference.

[0064] In the conventional digital signal transmission apparatus of the OFDM modulation system, the number of carriers is fixed and according the bandwidth is fixed.

[0065] Further, in the conventional transmission apparatus, when the transmission bandwidth is to be changed, there are many portions which must be changed in both of the transmission side and the receiving side. In addition, since the receiving side cannot follow the change of the bandwidth performed at the transmission side, the transmission bandwidth cannot be changed easily and in a moment.

[0066] According to the first embodiment of the present invention, the above drawbacks in the prior art can be removed and there can attain a transmission system which can change the bandwidth easily and perform exact bandwidth changing processing.

[0067] According to another embodiment of the present invention, the state of the transmission bandwidth is detected in the receiving side and the bandwidth mode in the receiving side is automatically changed.

[0068] The embodiment of the present invention described later comprises means for changing the following functional portions in interlocked relationship with one another in order to provide the bandwidth changeable transmission system by means of changing the number of carriers.

1) Function for changing an effective data output period and a frequency division ratio of the PLL/VCO 1-2 in the rate conversion unit 1;

2) Function for correcting a symbol amplitude and changing the period of the controller 2-5 for substituting the carrier amplitude with "0" in the coding unit 2T;

3) Function for changing the upper limit frequency and the lower limit frequency data of the ROMs 5-1 and 5-2 for generation of the SWEEP symbol in the synchronizing symbol insertion unit 5;

4) Function for changing the SWEEP symbol pattern stored in the memory included in the SWEEP calculation unit 4-2 in the synchronization detector 4;

5) Function for changing to shorten a period for decoding in the decoding unit 2R; and

6) Function for changing the frequency division ratio of the PLL/VCO and the period for taking in the effective data in the rate inverse-conversion unit 7.

[0069] Further, in another embodiment of the present invention, there is provided a data confirmation unit 18 supplied with data to be decoded and a controller for determining the state on the receiving side is controlled in accordance with an output of the data confirmation unit.

[0070] Namely, in the embodiment, the rate conversion unit 1 increases the frequency division ratio by N/G times and reduces the data taking-in amount per unit time by N/G times. Further, the effective data output period is reduced by N/G times. More particularly, after A (e.g. 688) symbol data have been outputted, the outputting is stopped temporarily and then A symbol data equal to a sum of (A+1)-th to 2A-th symbol data are outputted after the symbol period. This operation is made repeatedly.

[0071] The coding unit 2T prepares A sets of inputted data symbols and then produces an amplitude value "0" during the period that the rate conversion unit 1 is stopped temporarily. Further, in order to correct the reduced time waveform power prepared by the IFFT unit and caused by reduction by N/G times of the frequency component, the amplitude of the prepared symbol is increased to $1/(N/G)^2$. If the correction is not made, the electric power amount per symbol is changed when the synchronizing symbol group is compared with the data symbol group.

[0072] Consequently, when a signal passes through a digital processing unit having insufficient dynamic range or an analog unit left in the transmission system, the performance is deteriorated by a deteriorated S/N due to reduction of a signal level or clip. The deterioration of the performance can be avoided by the above-mentioned correction of the symbol amplitude.

[0073] The synchronizing symbol insertion unit 5 narrows the upper limit frequency and the lower limit frequency of data for the SWEEP symbol by N/G times in accordance with change of the bandwidth.

[0074] The SWEEP symbol pattern stored in the memory included in the SWEEP calculation unit 4-2 of the synchronization detector 4 is changed to narrow the upper limit frequency and the lower limit frequency by N/G times. Further, the period for decoding in the decoding unit 2R is shortened by N/G times to be A.

[0075] The effective data taking-in period of the rate inverse-conversion unit 7 is reduced by N/G times. More particularly, after A symbol data have been taken in, the taking-in operation is stopped temporarily and then A symbol data equal to a sum of (A+1)-th to 2A-th symbol data are taken in after the symbol period. This operation is made repeatedly.

[0076] Further, a frequency division ratio of the PLL/VCO is increased by G/N times and the output data amount per unit time is reduced by N/G times.

[0077] The above changing operation can effect realization of the taking-in output clock rate corresponding to the transmission rate varied due to change of the bandwidth, prevention of the output level variation due to change of the number of carriers and maintenance of the synchronization accuracy due to use of the SWEEP symbol using the bandwidth changing from end to end throughout.

[0078] Further, operation of another embodiment of the present invention is now described.

[0079] Components of all the bandwidths to be subjected to the FFT in the frequency components subjected to the FFT transform are arranged to be outputted successively as shown by Rf of Fig. 22.

[0080] Accordingly, the output arrangement of components having the output level equal to zero can be confirmed to thereby decide the number of carriers prepared on the transmission side. A mode for decoding or inverse-conversion processing of the data rate is determined on the basis of the result of the decision.

[0081] A bandwidth changeable transmission system in which the number of carriers is changed according to an embodiment of the present invention is now described with reference to Fig. 1 schematically illustrating the overall configuration thereof in a block diagram.

[0082] In the transmission side, an output terminal of a clock generator 11 is connected to respective clock terminals CK of a rate conversion unit 1, a coding unit 2T, an IFFT unit 3A, a guard addition unit 3B, a synchronizing symbol insertion unit 5 and an orthogonal modulation processing unit 8. Change control signals CNT1A to CNT1E from a controller 13T are supplied to control input terminals of the rate conversion unit 1, the coding unit 2T and the synchronizing symbol insertion unit 5, respectively. The controller 13T designates respective operation modes of the rate conversion unit 1, the coding unit 2T and the synchronizing symbol insertion unit 5.

[0083] In the receiving side, an output VC of a synchronization detector 4 is connected to a terminal VC of a voltage controlled clock generator 12. An output FSTr of the synchronization detector 4 is connected to respective FST termi-

nals of an FFT unit 3C and a rate inverse-conversion unit 7. An output CKr of the voltage controlled clock generator 12 is connected to respective clock terminals of the FFT unit 3C, the rate inverse-conversion unit 7, an orthogonal demodulation processing unit 9 and the synchronization detector 4. Change control signals CNT2F to CNT2H from a controller 13R are supplied to the rate inverse-conversion unit 7, a decoding unit 2R and the synchronization detector 4.

[0084] A definite configuration of the synchronization detector 4 used in the present invention is now described with reference to Fig. 11.

[0085] Input signals R'sg and I'sg are supplied to an end-of-NULL detector 4-1 and a SWEEP calculation unit 4-2. A SWEEP period flag pulse produced by the end-of-NULL detector 4-1 is supplied to an ST terminal of the SWEEP calculation unit 4-2. Respective CK terminals of the end-of-NULL detector 4-1, the SWEEP calculation unit 4-2 and a frame counter 4-4 are supplied with a clock CKr. A coincidence pulse produced by the SWEEP calculation unit 4-2 is inputted to an R terminal of a PLL 4-5.

[0086] Further, an output FSTr of the frame counter 4-4 which counts 1056x400 clocks CKr is supplied to subsequent circuits connected thereto and a V terminal of the PLL 4-5. The PLL 4-5 produces a signal VC having a voltage varying depending on a phase of a signal inputted to the V terminal and an R terminal thereof.

[0087] The voltage controlled clock generator 12 increases or decreases the frequency of the clock CKrc produced thereby in accordance with a magnitude of a voltage of the signal VC supplied from the synchronization detector 4.

[0088] A definite configuration of the rate conversion unit 1 used in the embodiment of the present invention is now described with reference to Fig. 8. The inputted clock CK is supplied to a change-over type PLL/VCO 1-2 and the PLL/VCO 1-2 produces a clock CKm having the frequency equal to N/G times of the clock CK. Further, the clock CK is supplied to an FST counter 1-4, which produces the FST pulse which is a frame reference in processing of the transmission side. The FST pulse from the FST counter 1-4 is supplied to WRST and RRST terminals of an FIFO memory 1-3 as a reference of reset. Reading of data from the FIFO memory 1-3 is made on the basis of a level at an RE terminal in synchronism with the clock of the RCK terminal.

[0089] A pulse to the RE terminal is supplied from a change-over type decoder 1-5. The decoder 1-5 is supplied with a counter address value form the FST counter 1-4 and changes a decoding condition in response to the control signal CNT1B to change an RE pulse output period.

[0090] The inputted serial data Din is supplied to a serial-to-parallel (S/P) converter 1-1 to be converted into a parallel signal, which is inputted to the FIFO memory 1-3. The change-over type PLL/VCO 1-2 is supplied with the control signal CNT1A and changes a frequency division ratio of the clock to be outputted in response to the control signal CNT1A.

[0091] An definite configuration of the coding unit 2T used in the embodiment of the present invention is now described with reference to Fig. 9. The inputted signal Dii is supplied to mapping ROMs 2-1 and 2-2 in which the signal Dii is converted into signals at predetermined points of I and Q axes. The outputs of the ROMs 2-1 and 2-2 are supplied to selectors 2-3 and 2-4. Outputs produced by the selectors 2-3 and 2-4 are outputted through amplitude changing units 2-6 and 2-7.

[0092] The control signal CNT1D is inputted to control terminals of the amplitude changing units 2-6 an 2-7. A change pulse produced by the change-over type controller 2-5 is supplied to input selection terminals of the selectors 2-3 and 2-4. The control signal CNT1C is supplied to the change-over type controller 2-5 to change the decoding condition for preparation of the change pulse.

[0093] Signals in the period corresponding to the unnecessary carriers described above (Fig. 5) are substituted with "0" in the selectors 2-3 and 2-4 to thereby produce the signals Rf and If.

[0094] Configuration of the synchronizing symbol insertion unit 5 used in the embodiment of the present invention is now described with reference to Fig. 10. ROms 5-1 and 5-2 controlled by a controller 5-5 having the timing determined by the clock CK and the FST pulse produce the synchronizing symbol signals at the timing according to the FST pulse. Similarly, selectors 5-3 and 5-4 controlled by a controller 5-6 having the timing determined by the clock CK and the FST pulse select the synchronizing symbol signals from the ROMs 5-1 and 5-2 only during one to four symbol periods, which are the no-signal periods in the current stage, of the prepared guard-added time signals Rg and Ig and output the selected signals.

[0095] The control signal CNT1E is inputted to upper-part address terminals of the ROMs 5-1 and 5-2 so that the SWEEP symbol patterns having different upper limit and lower limit frequencies are selected to be outputted.

[0096] An definite configuration of the decoding unit 2R used in the embodiment of the present invention is now described with reference to Fig. 12. Input signals R'f and I'f are supplied to address terminals of an ROM 2R-1 and a differential detector 2R-3. An output D'o from the ROM 2R-1 is outputted from an output terminal and is supplied to the differential detector 2R-3. An output of the differential detector 2R-3 is supplied to an accumulator 2R-4. An EN terminal of the accumulator 2R-4 is supplied with an SGC signal supplied from a controller 2R-2 and indicating the data period for decoding.

[0097] The differential detector 2R-3 calculates a differential vector of an originally existing signal point on mapping, identified by the ROM 2R-1 and signal points of R'f and I'f inputted to the decoding unit 2R.

[0098] The accumulator 2R-4 takes in the differential vector on the basis of the SGC signal only during the period that

carriers exist in the signal of the bandwidth which is frequency-converted by the FFC 3C. The controller 2R-2 changes the SGC signal indicating the data period for decoding in response to the control signal CNT2G on the basis of the clock CKrc and the pulse FSTrc.

[0099] Configuration of the rate inverse-conversion unit 7 used in the embodiment of the present invention is now described with reference to Fig. 13. The input signal D'o is connected to a Din terminal of an FIFO memory 7-3. An output of a decoder 7-2 is connected to a WE terminal for controlling writing. The decoder 7-2 changes a signal period to the WE terminal on the basis of the control signal CNT2G. A PLL/VCO 7-4 changes a frequency division ratio of the clock in accordance with the control signal CNT2H. Consequently, the mode for rate inverse-conversion is changed.

[0100] The timing operation of the rate conversion unit 1 and the rate inverse-conversion unit 7 described above is shown in Fig. 5 and difference in frequency component upon changing of the number of carriers is shown in Fig. 6.

[0101] In Fig. 6, the ordinate axis represents the frequency and the hatched portion represents an effective signal area. Symbols n, m and L are any positive integers. (a) in Fig. 6 shows the case where the number m of carriers is set so that all of the frequency bandwidths to which the transmission signal is given are used. (b) in Fig. 6 shows the case the number of carriers is changed to n smaller than m and the bandwidth of the transmission signal is reduced as compared with the case of (a). (c) in Fig. 6 shows the case where the number of carriers is change to L smaller than m to reduce the bandwidth of the transmission signal to a half and the carrier frequency is shifted to the lower side. In the case of (c), another channel having the same transmission bandwidth in the higher frequency side can be set.

[0102] A bandwidth changeable transmission system according to a second embodiment of the present invention is now described with reference to Fig. 2 schematically illustrating the overall configuration thereof in a block diagram.

[0103] The FSTrc signal of the synchronization detector 15 is supplied to an FST terminal of the data confirmation unit 18 and the clock CKrc is supplied to a CK terminal of the data confirmation unit 18. The outputs R'f and I'f of the FFT unit 3C are supplied to D terminals of the data confirmation unit 18. An output Px of the data confirmation unit 18 is supplied to a control terminal of a controller 13RC.

[0104] Overall operation of the embodiment is now described.

[0105] When the carriers are set to be N/G times in the controller 13T at the transmission side, the number of carriers, the SWEEP synchronizing symbol range and the like are changed and the transmission bandwidth is also changed to N/G times.

[0106] At this time, the FFC unit 3C at the receiving side produces the frequency components of the bandwidth determined by the number of FFT samples and the sampling frequency successively.

[0107] Accordingly, the bandwidth being used for transmission and hence the number of carriers is confirmed by detecting the position of the carrier having the level of "0". More particularly, since the components of carriers appear from the FFT unit 3C, the timing that the level 0 is started may be counted on the basis of the FSTrc signal or the like.

[0108] Namely, the data confirmation unit 18 examines the states (level) of the signals R'f and I'f and sends a Px signal indicating change of the bandwidth at the transmission side to the controller 13RC.

[0109] Respective operation modes of the synchronization detector 15, the decoding unit 2R and the rate inverse-conversion unit 7 are changed to the number of carriers corresponding to the change of the bandwidth at the transmission side in accordance with the control signals CNT2F to CNT2H from the controller 13RC.

[0110] Referring now to Figs. 23A, 23B and 23C, operation and configuration of the data confirmation unit 18 of the receiver 104 are described in detail.

[0111] Fig. 23A shows the frequency distribution of the IFFT output at intervals of carriers of about 20 KHz using the frequency CKd of 20 MHz at the transmission side and an example where the frequency component of the received signal is sampled at intervals of about 10 KHz using the frequency CKr of 10 MHz at the receiving side. The sample frequency intervals of carriers at the transmission side are not coincident with the sample frequency intervals of carriers at the receiving side. Accordingly, no-component portions represented by "-" appear alternately in the output R'f of the FFT unit 3 indicating the frequency component of the received signal and furthermore the components also appear alternately in the sixth and subsequent outputs R'f which have no carrier originally.

[0112] Fig. 23B shows the frequency distribution of the IFFT output at intervals of carriers of about 10 KHz using the frequency CKd of 10 MHz at the transmission side and an example where the frequency component of the received signal is sampled at intervals of about 20 KHz using the frequency CKr of 20 MHz at the receiving side. Similarly, the sample frequency intervals of carriers at the transmission side are not coincident with the sample frequency intervals of carriers at the receiving side. Accordingly, the frequency components "1", "3" and the like of the received signal are not sampled and no-component portions represented by "-" appear in the fifth and previous outputs which have carriers originally.

[0113] Fig. 23C schematically illustrates the data confirmation unit 18 for five carriers. Whether the input signal includes components corresponding to transmission carriers or not is examined by a comparator 18-1. When the input signal includes no component as represented by "-", the input signal is successively inputted to a shift register 18-2 as a level H. A "-" detection gate produces an output H when contents at third and subsequent stages are H and correspond to the data symbol period in order to detect the state shown in Fig. 23B. A "-" detection gate 18-4 produces an

output H when contents at odd stages and correspond to the data symbol period in order to detect the state shown in Fig. 23A.

[0114] In the case of Figs. 26A and 26B, since contents at fifth and previous stages as counted from left are set to a level L, both the "-" detection gates 18-3 and 18-4 do not produce any operation output H.

[0115] Operation in case where the number of carriers is changed while maintaining the number of information symbols as it is has been described in the foregoing.

[0116] A bandwidth changeable transmission system according to a third embodiment of the present invention is now described with reference to Fig. 3 illustrating the overall configuration thereof in a block diagram. The bandwidth changeable transmission system is to change the number of carriers every symbol and substitutes a rate conversion unit 1Y, a coding unit 2TY, a decoding unit 2RY and a rate inverse-conversion unit 7Y for the rate conversion unit 1, a coding unit 2T, a decoding unit 2R and the rate inverse-conversion unit 7 of Fig. 2, respectively.

[0117] Operation thereof is now described with reference to Figs. 5 to 7.

[0118] In the embodiment, the RE pulse and "0" substitution period, the period for accumulation and the WE pulse period are modified to be outputted at only the first half of the frame signal. The configuration is effective when it is applied to the case where the time allocation period of the transmission signal is modified in the time-division transmission or the like.

[0119] Fig. 6(a) shows the state of frequency components which are divided into two high and low parts in the center of the channel frequency and occupy all the bandwidths. Fig. 6(b) shows the state of frequency components which are divided into two high and low parts in the center of the channel frequency and in which the number of carriers is deleted so that all the bandwidths are not occupied but part of the bandwidths are occupied. Fig. 6(c) shows the state of frequency components in which the number of carriers is deleted so that all the bandwidths are not occupied but part of the bandwidths are occupied and the channel frequency is shifted to any of high and low parts from the center.

[0120] Fig. 4 schematically illustrates an automatic bandwidth changeable transmission system to which the present invention is applied.

[0121] A circuit state monitoring apparatus 106 examines the use state of electric wave in a circuit to be used and determines a frequency to be used and a usable bandwidth in accordance with the empty state thereof, so that a change control signal S1 is produced to be supplied to a control terminal of a bandwidth changeable modulation apparatus 101. Further, the monitoring apparatus 106 produces a change control signal S2 to be supplied to a control terminal of a frequency conversion transmission apparatus 102.

[0122] The bandwidth changeable modulation apparatus 101 and the frequency conversion transmission apparatus 102 constitute in large blocks the transmission side shown in Figs. 1, 2 and 3 and the bandwidth changeable modulation apparatus 101 corresponds to the rate conversion unit 1 to the synchronizing symbol insertion unit 5 while the frequency conversion transmission apparatus 102 corresponds to the orthogonal modulation processing unit 8. The apparatuses include the function of capable of controlling the change externally.

[0123] Further, a bandwidth changeable demodulation apparatus 104 sends to a frequency conversion reception apparatus 103 a change control signal S3 from the demodulation state such as the presence of carriers.

[0124] The frequency conversion reception apparatus 103 and the bandwidth changeable demodulation apparatus 104 constitute in large blocks the receiving side shown in Figs. 1, 2 and 3 and the frequency conversion reception apparatus 103 corresponds to the orthogonal demodulation processing unit 9 and the bandwidth changeable demodulation apparatus 104 corresponds to the FFT unit 3 to the rate inverse-conversion unit 7.

[0125] Operation of the system is now described.

[0126] Prior to the start of transmission, the circuit state monitoring apparatus 106 at the transmission side examines the use state of electric wave for a circuit to be used and determines a frequency to be used and a usable bandwidth in accordance with the empty state of the circuit.

[0127] The bandwidth to be used is designated to the bandwidth changeable modulation apparatus 101 by means of the change control signal S1 and the frequency to be used is designated to the frequency conversion transmission apparatus 102 by means of the change control signal S2.

[0128] The bandwidth changeable modulation apparatus 101 changes the number of carriers as described above so that the bandwidth to be used is set. Further, the frequency conversion transmission apparatus 102 controls the local oscillation frequency so that the frequency to be used is set. Thus, the transmission signal having the frequency to be used and the bandwidth to be used is transmitted to the receiving side.

[0129] On the other hand, the bandwidth changeable modulation apparatus 104 at the receiving side decides whether the current state corresponds to any of the state that all carriers are present, the state that only part of carriers are present and the approximately expected carriers are present and produces the change control signal S3 corresponding to the decided state to be supplied to the frequency conversion reception apparatus 103.

[0130] The frequency conversion reception apparatus 103 changes the reception frequency in accordance with the change control signal S3 so that the apparatus 103 can receive the transmission signal from the transmission side.

[0131] As configured above, there can structure the system which searches for an empty channel automatically and

transmits data with the transmission bandwidth corresponding to the empty bandwidth.

[0132] More particularly, usually, in the transmission system using the transmission channel interval of 18 MHz and including the combined frequency conversion transmission apparatus 102 and frequency conversion reception apparatus 103, the scheme shown in Fig. 6(b) is used to shift the frequency to the upper side by a half channel in the frequency conversion transmission apparatus 102 to be outputted while in another frequency conversion transmission apparatus 102 the scheme shown in Fig. 6(b) is also used to shift the frequency to the lower side by a half channel to be outputted, so that signals for two channels can be transmitted by means of one transmission bandwidth.

[0133] Fig. 24 schematically illustrates an example of a circuit state monitoring apparatus 106. Detection signals from a group of receivers 106-1 indicating the use state of electric wave having the usable frequency bandwidth are supplied to a group 106-2 of ANDs 2 and a priority encoder 106-5. Outputs D1 to DN of the group of ANDs 2 are supplied to an OR.N and a priority encoder 106-4. An output of the OR.N is outputted as a change control signal 1 and is supplied to a control terminal of a SEL 106-6. The SEL 106-6 selects an output of the priority encoder 106-4 to be produced as a change control signal 2 when all of any one channel is empty and the output of the OR.N is high. Further, when all of any one channel is not empty but only a half channel is empty and the output of the OR.N is low, the SEL 106-6 selects an output of the priority encoder 106-5 to be produced as the change control signal 2. The priority encoder decides an output with preference to the presence of the leftmost signal in the drawing among the inputted signals. For example, when the leftmost signal D:1L is present, the same output is decided even if all other inputs are present and all other inputs are not present. Thus, it is judged that the leftmost channel is empty to determine the frequency to be used.

[0134] According to the embodiments of the present invention described above, there can realized the transmission apparatus in which the number of carriers can be changed at the transmission side to change the bandwidth and the change of the bandwidth can be followed at the receiving side automatically.

[0135] A further embodiment of an OFDM modulation system which can change the frequency bandwidth for a transmission signal according to the present invention is now described with reference to the drawings. In the embodiment described below, the clock frequency is changed to thereby change the frequency interval between adjacent carriers so that the whole transmission frequency bandwidth is changed.

[0136] In the embodiment to be described below, the rate of the clock supplied to each portion is changed at the transmission side, and at the receiving side the synchronizing signal detected from the received signal is phase-compared with the frame signal prepared by frequency-dividing the clock at the receiving side. The clock frequency of the receiving side clock oscillator is controlled in accordance with the compared result and the bandwidth to be demodulated at the receiving side is caused to follow the bandwidth at the transmission side automatically so that the transmission bandwidth is changed.

[0137] More particularly, in the IFFT transform at the transmission side, the n-th data fn determines an amplitude level at the period 1024/(n S) of the n-th carrier. In this connection, when the period of the clock supplied to the IFFT transform unit is changed, the frequency of the n-th carrier is also changed. The transmission bandwidth is determined by the maximum frequency of the generated carrier.

[0138] Namely, change of the bandwidth can be realized by changing the period of the clock. Further, by changing the period of the clock, the symbol period is also changed and the frame period determined by the number of symbol is also changed.

[0139] At the receiving side, the period of the SWEEP symbol and the NULL symbol detected from the received signal, that is, the frame period at the transmission side is compared with the FSTr period defined in the frame counter and the period of the clock at the receiving side is controlled to minimize the difference therebetween. Thus, there can structure the transmission system which can automatically follow the bandwidth changing processing performed at the transmission side.

[0140] The bandwidth changing transmission system of the embodiment is now described with reference to Fig. 25 schematically illustrating the overall configuration thereof in a block diagram.

[0141] At the transmission side, the clock output terminal of the clock oscillator 11 is connected to a clock rate conversion unit 10. A clock output terminal of the clock rate conversion unit 10 is connected to the respective clock terminals of the rate conversion unit 1, the coding unit 2T, the IFFT unit 3A, the guard addition unit 3B, the synchronizing symbol insertion unit 5 and the orthogonal modulation processing unit 8.

[0142] At the receiving side, the output VC of the synchronization detector 15 is connected to the terminal VC of the voltage controlled clock oscillator 12. The output FSTr of the synchronization detector 15 is connected to the respective FST terminals of the FFT unit 3C and the rate inverse-conversion unit 7. The output CKr of the voltage controlled clock oscillator 12 is connected to the respective clock CK terminals of the FFT unit 3C, the rate inverse-conversion unit 7, the orthogonal demodulation processing unit 9 and the synchronization detector 15.

[0143] The bandwidth changeable processing operation at the transmission side is first described.

[0144] When the transmission bandwidth is changed, the clock rate conversion unit 10 changes the clock CK from the clock oscillator 11 to the clock having the rate corresponding to the bandwidth to be changed. That is, the clock rate conversion unit 10 produces the clock CKd having the rate equal to V times the rate of the clock CK.

[0145] Since the frame period pulse FST produced by the rate conversion unit 1 is outputted every counting of, for example, 1056×400 clocks CKd, the coding unit 2T, the IFFT unit 3A, the guard addition unit 3B, the synchronizing symbol insertion unit 5 and the orthogonal modulation processing unit 8 which are operated on the basis of the clock CK and the frame period pulse FST produce the output data having the sample rate changed to (V/NR) times during the period changed to (NR/V) times.

[0146] Further, since the rate of the clock CK inputted to the PLL/VCO 1-2 (Fig. 8) in the rate conversion unit 1 is changed to V times, the rate of N/G of the clock CKm is also changed to (V/NR) times and the rate of the taken-in data Din is also changed to (V/NR) times.

[0147] The case where (V/NR) is equal to, for example, 1/2 is described. In this case, when the rate of the sample clock CKd in the IFFT unit 3A is set to 1/2, the interval of carriers is set to 1/2 and the symbol period is increased to two times.

[0148] At this time, since the bandwidth is determined on the basis of the product of the carrier interval and the number of carriers and the number of carriers is not changed, the bandwidth is reduced to a half in this example where (V/NR) is 1/2.

[0149] Namely, the clock rate can be set to (V/NR) times to thereby change the bandwidth to (V/NR) times.

[0150] Change of the bandwidth by changing the frequency CKd is now described by taking as an example the case where the number of carriers is 5 for simplification of description. Fig. 26A shows the frequency component distribution of the IFFT output at intervals between carriers of about 20 KHz using the frequency CKd of 20 MHz at the transmission side and an example where the frequency component of the received signal is sampled at intervals of about 20 KHz using the frequency CKr of 20 MHz at the receiving side. The frequency component distribution of the time waveform R produced by the IFFT 3A is shown at the upper side of Fig. 26A and a series of data R'f having the frequency component obtained in the FFT unit 3C by receiving the OFDM wave prepared from the time waveform R or the like is shown.

[0151] Fig. 26B shows the frequency distribution of the IFFT output at intervals of carriers of about 10 KHz using the frequency CKd of 10 MHz at the transmission side and an example where the frequency component of the received signal is sampled at intervals of about 10 KHz using the frequency CKr of 10 MHz at the receiving side. The sample frequency intervals of carriers at the transmission side are coincident with the sample frequency intervals of carriers at the received side are coincident. Further, since no clear frequency component appear in sixth and subsequent received data string in which any carrier is not set, "-" in Figs. 26A and 26B shows no frequency component.

[0152] The bandwidth change processing operation at the receiving side is now described.

[0153] The synchronization detector 15 searches for the SWEEP symbol on the basis of the NULL period detected from the inputted signals R'sg and I'sg as described above and phase-compares the SWEEP symbol with the coincidence pulse indicating the reception frame period to control the frequency of the clock CKrc. Further, the synchronization detector 15 produces the frame period pulse FSTrc prepared by counting, for example, 1056×400 clocks CKrc.

[0154] Since the FFT unit 3C and the rate inverse-conversion unit 7 are operated by the pulse FSTrc and the clock CKrc, the coincidence pulse for a reference of the phase comparison with the pulse FSTrc has the period equal to NR/V times when the sample rate at the transmission side is multiplied by V/NR and accordingly when the clock CKrc is changed to the frequency equal to V/NR times the usual frequency, the frequencies and the phases of the pulse FSTrc and the coincidence pulse are coincident with each other.

[0155] A definite configuration of the synchronization detector 15 is now described with reference to Fig. 27. The inputted signals R'sg and I'sg are supplied to the end-of-NULL detector 15-1 and the SWEEP calculation unit 15-2. The SWEEP flag pulse produced by the end-of-NULL detector 15-1 is supplied to the ST terminal of the SWEEP calculation unit 15-2.

[0156] The clock CKrc is supplied to the respective terminal CK terminals of the end-of-NULL detector 15-1, the SWEEP calculation unit 15-2 and the frame counter 15-4.

[0157] The coincidence pulse produced by the SWEEP calculation unit 15-2 is supplied to an R terminal of a PLL 15-3.

[0158] Further, the FSTrc of the frame counter 15-4 which counts 1056×400 clocks CKrc is inputted to a subsequent circuit connected to the output of the frame counter and a V terminal of the PLL 15-3.

[0159] The PLL 15-3 produces a signal VC of which a voltage is varied in accordance with a phase of the pulse inputted to the V and R terminals thereof.

[0160] The voltage controlled clock generator 12 increases or decreases the frequency of the clock CKrc produced thereby in accordance with a magnitude of a voltage of the signal VC supplied from the synchronization detector 15, that is, in accordance with the clock rate conversion of the clock CKd at the transmission side.

[0161] With the above processing, the clock CKrc and the frame period pulse FSTrc used at the receiving side can follow the clock CKd and the frame period pulse FST changed at the transmission side.

[0162] A second embodiment of the bandwidth changeable transmission system using change of the clock is schematically illustrated in Fig. 28 in a block diagram and portions different from Fig.25 are now described mainly.

[0163] An output clock CKrc of a clock oscillator 16 at the receiving side is supplied to a clock rate conversion unit 17. An output clock CKrc of the clock rate conversion unit 17 are supplied to the respective CK terminals of the FFT unit 3C, the rate conversion unit 7 and the data confirmation unit 18.

[0164] The FST terminal of the data confirmation unit 18 is supplied with the pulse FSTrc of the synchronization detector 15 and the D terminal of the data confirmation unit is supplied with the D'o of the coding unit 2R.

[0165] As described above, when the transmission bandwidth at the transmission side is set to V/NR (for example, 1), the number of carriers is not changed and accordingly the interval of carrier is V/NR.

[0166] When the FFT transform operation is performed with the original clock rate at the receiving side, that is, when the FFT transform operation is performed as the carrier interval is maintained to a half, the output D'o obtained from the decoding unit 2R as the result thereof becomes a toothless state in which "0" is set alternately. Further, on the contrary, when the FFT transform operation is performed with the clock rate at the transmission side being a half and the clock rate at the receiving side being one time, the output D'o obtained from the decoding unit 2R is set in the state that there is no data of carriers having a higher frequency.

[0167] Accordingly, the data confirmation unit 18 examines the state of the output D'o to confirm the change state of the clock rate at the transmission side.

[0168] The data confirmation unit 18 produces a control signal for instructing change of the clock rate to be supplied to the clock rate conversion unit 17 so that the clock rate at the receiving side is equal to the clock rate corresponding to the change of the clock rate at the transmission side.

[0169] Consequently, the clock rate conversion unit 17 changes the clock CKrc at the receiving side to the clock rate corresponding to the change of the clock rate at the transmission side in response to the control signal supplied from the data confirmation unit 18.

[0170] In this connection, by changing the clock rate at the transmission side to a half, a third or the like simply, false detection in the confirmation operation of the data confirmation unit 18 at the receiving side can be reduced.

[0171] With the configuration described above, the clock CKrc and the frame period pulse FSTrc used at the receiving side can follow the clock CKd and the frame period pulse FST changed at the transmission side.

[0172] Fig. 29 is a block diagram schematically illustrating a third embodiment of a bandwidth changeable transmission system using change of the clock frequency. The embodiment of Fig. 29 includes the rate conversion unit 17 and the data confirmation unit 18 in addition to the configuration of Fig.25 and description of operation thereof is omitted.

[0173] The clock rate conversion units 10 and 17 have only the function for changing the clock rate to a half, a third, a fourth or the like by only the frequency division operation using logic elements. This configuration is mainly used when the clock rate can change only in the range that the change width of frequency of the voltage controlled clock oscillator 12 at the receiving side is narrow.

[0174] Fig. 30 schematically illustrates an automatic bandwidth changeable transmission system to which the present invention is applied.

[0175] A circuit state monitoring apparatus 106 examines the use state of electric wave in a circuit to be used and determines a frequency to be used and a usable bandwidth in accordance with the empty state thereof and is configured as shown in Fig. 24. The monitoring apparatus 106 produces a change control signal S1 to be supplied to a control terminal of a bandwidth changeable modulation apparatus 201. Further, the monitoring apparatus 106 produces a change control signal S2 to be supplied to a control terminal of a frequency conversion transmission apparatus 202.

[0176] The bandwidth changeable modulation apparatus 201 and the frequency conversion transmission apparatus 202 constitute in large blocks the transmission side shown in Figs. 25, 28 and 29 and the bandwidth changeable modulation apparatus 201 corresponds to the rate conversion unit 1 to the synchronizing symbol insertion unit 5 while the frequency conversion transmission apparatus 202 corresponds to the orthogonal modulation processing unit 8. The apparatuses include the function for capable of controlling the change externally.

[0177] Further, a bandwidth changeable demodulation apparatus 204 sends to a frequency conversion reception apparatus 203 a change control signal S3 from the demodulation state such as the presence of carriers.

[0178] The frequency conversion reception apparatus 203 and the bandwidth changeable demodulation apparatus 204 constitute in large blocks the receiving side shown in Figs. 25, 28 and 29 and the frequency conversion reception apparatus 203 corresponds to the orthogonal demodulation processing unit 9. The bandwidth changeable demodulation apparatus 204 corresponds to the FFT unit 3 to the rate inverse-conversion unit 7.

[0179] Operation of the system is now described.

[0180] Prior to the start of transmission, the circuit state monitoring apparatus 206 at the transmission side examines the use state of electric wave for a circuit to be used and determines a frequency to be used and a usable bandwidth in accordance with the empty state of the circuit.

[0181] The bandwidth to be used is designated to the bandwidth changeable modulation apparatus 201 by means of the change control signal S1 and the frequency to be used is designated to the frequency conversion transmission apparatus 202 by means of the change control signal S2.

[0182] The bandwidth changeable modulation apparatus 201 changes the clock rate as described above so that the

bandwidth to be used is set. Further, the frequency conversion transmission apparatus 202 controls the local oscillation frequency so that the frequency of the clock is set to the frequency to be used. Thus, the transmission signal having the frequency to be used and the bandwidth to be used is transmitted to the receiving side.

[0183] On the other hand, the bandwidth changeable modulation apparatus 204 at the receiving side decides whether the current state corresponds to any of the state that all carriers are present, the state that only part of carriers are present and the approximately expected carriers are present and produces the change control signal S3 corresponding to the decided state to be supplied to the frequency conversion reception apparatus 203.

[0184] The frequency conversion reception apparatus 203 changes the reception frequency in accordance with the change control signal S3 so that the apparatus 203 can receive the transmission signal from the transmission side.

[0185] As described above, there can structure the system which automatically search for an empty channel and performs data transmission with the transmission bandwidth corresponding to the empty bandwidth.

[0186] Fig. 31 shows a relation of the frame period time in case where the clock rate is set to one time and the frequency component in this case. Further, Fig. 32 shows a relation of the frame period time in case where the clock rate is increased and the frequency component in this case.

[0187] As described above, when the clock rate is reduced to a half, the frame period is increased to two times but the frequency bandwidth is reduced to a half.

[0188] Accordingly, the bandwidth for one channel can be utilized in the case of Fig. 31 and another channel can be utilized in the case of Fig. 32.

[0189] Namely, in the transmission system shown in Fig. 30, there can be combined the frequency conversion transmission apparatus 202 and the frequency conversion reception apparatus 203 which can change the transmission and reception frequencies in a half channel unit.

[0190] Thus, the bandwidth of one channel can be utilized for a plurality of transmissions, so that a limited transmission bandwidth can be utilized effectively.

[0191] According to the embodiment described above, there can be realized the system in which the clock rate can be changed at the transmission side to thereby change the bandwidth and the receiving side can follow the change automatically.

Claims

1. A communication method in an orthogonal frequency division multiplexing modulation communication system, comprising the steps of:

   changing, in a transmission apparatus, a setting of frequency bandwidth of a signal which was modulated in accordance with an orthogonal frequency division multiplexing modulation method to a predetermined bandwidth within a bandwidth allocated to said communication system;
   transmitting said modulated signal; and
   receiving, in a receiving apparatus, said modulated transmission signal and changing a setting of demodulation frequency bandwidth of said received signal to follow the change of said frequency bandwidth of said modulated signal.

2. A communication method according to Claim 1, wherein the setting change of said frequency bandwidth of said modulated signal is made by changing the number of carriers of said transmission signal.

3. A communication method according to Claim 2, wherein said changing step of the number of carriers includes the steps of:

   changing an amount of input data per unit time in said transmission apparatus;
   changing an effective data period of said modulated signal;
   changing a pattern of a synchronizing signal added to said modulated signal; and
   changing a transmission signal level to satisfy a transmission condition.

4. A communication method according to Claim 3, comprising performing, in accordance with the change of the number of carriers in said transmission apparatus, the steps of:

   changing a reference signal pattern for synchronization detection in said receiving apparatus to detect the synchronizing signal from said received signal;
   changing an effective data period of a signal obtained by decoding said received signal; and
   changing a taking-in period of data component in said effective data period.

5. A communication method according to Claim 3, wherein the number of carrier signals is detected from said received signal and when it is detected that the number of carriers is changed, a control signal for indicating change of a reference signal pattern for synchronization detection in said receiving apparatus, change of an effective data period of a signal obtained by decoding said received signal, and change of a taking-in period of data component in said effective data period is produced.

6. A communication method according to Claim 3, further comprising the steps of:

producing a control signal for changing the setting of frequency bandwidth of said transmission signal to a predetermined bandwidth; and
changing the setting of frequency bandwidth of said signal modulated in accordance with the orthogonal frequency division multiplexing modulation method in accordance with said control signal.

7. A communication method according to Claim 1, wherein the setting change of said frequency bandwidth of said modulated signal is made by changing a frequency of a clock signal in said transmission apparatus.

8. A communication method according to Claim 7, wherein the setting change of said frequency bandwidth of said modulated signal is detected on the basis of said received signal and a frequency of a clock signal in said receiving apparatus is changed in accordance with the detected change of said frequency bandwidth to thereby change said demodulation frequency bandwidth.

9. A communication method according to Claim 8, wherein said modulated signal includes a synchronizing signal and said synchronizing signal is detected from said received signal, a phase of said detected synchronizing signal being compared with a phase of a reference signal prepared on the basis of a current clock signal in said receiving apparatus so that said frequency of said clock signal in said receiving apparatus is changed in accordance with a phase difference.

10. A communication method according to Claim 8, wherein when an interval between adjacent carrier signals of said modulated signal is changed in accordance with the change of said frequency of said clock signal in said transmission apparatus and said received signal is decoded, omission of said carrier signals is detected and said frequency of said clock signal in said receiving apparatus is controlled to dissolve the omission of said carrier signals.

11. A communication method according to Claim 10, wherein said changing step of said frequency of said clock signal in said receiving apparatus includes the steps of changing said frequency by a first change amount and a step of changing said frequency by a second change amount smaller than said first change amount.

12. A communication method according to Claim 9, comprising controlling a phase of said clock signal together with the change of said frequency of said clock signal in said receiving apparatus.

13. A communication method according to Claim 7, further comprising the steps of:

producing a control signal for changing said frequency bandwidth of said signal to be transmitted; and
changing said setting of frequency bandwidth of said signal modulated with the orthogonal frequency division multiplexing modulation method in accordance with said control signal.

14. A communication method according to Claim 1, wherein said orthogonal frequency division multiplexing modulation system is a digital modulation system for at least one wave of carriers being a quadrature amplitude modulation system.

15. A transmission method in an orthogonal frequency division multiplexing modulation communication system, comprising the steps of:

changing a setting of frequency bandwidth of a signal which was modulated in accordance with an orthogonal frequency division multiplexing modulation method to a predetermined bandwidth within a bandwidth allocated to said communication system by changing the number of carriers of said signal; and
transmitting said modulated signal.

16. A transmission method according to Claim 15, wherein said changing step of said number of carriers includes the

steps of:

changing an amount of input data per unit time in said transmission apparatus;
changing an effective data period of said modulated signal;
changing a pattern of a synchronizing signal added to said modulated signal; and
changing a transmission signal level to satisfy a transmission condition.

17. A transmission method in an orthogonal frequency division multiplexing modulation communication system, comprising the steps of:

changing a frequency bandwidth of a signal modulated in accordance with an orthogonal frequency division multiplexing modulation method to a predetermined bandwidth within a bandwidth allocated to said communication system by changing a frequency of a clock signal in said transmission apparatus; and
transmitting said modulated signal.

18. A receiving method in an orthogonal frequency division multiplexing modulation communication system, comprising the steps of:

receiving, in a receiving apparatus, an orthogonal frequency division multiplexing modulated signal having a changed bandwidth; and
changing a demodulation frequency bandwidth of said received signal to follow change of a frequency bandwidth of said modulated signal;
said changing step of said demodulation frequency bandwidth further including the steps of:
changing a reference signal pattern for synchronization detection in said receiving apparatus to detect a synchronizing signal from said received signal;
changing an effective data period of a signal obtained by decoding said received signal and
changing a taking-in period of data component in said effective data period.

19. A receiving method according to Claim 18, wherein the number of carriers is detected from said received signal and when it is detected that the number of carriers is changed, a control signal for indicating change of said reference signal pattern for synchronization detection in said receiving apparatus, change of said effective data period of a signal obtained by decoding said received signal, and change of said taking-in period of the data component in said effective data period is produced.

20. A receiving method in an orthogonal frequency division multiplexing modulation communication system, comprising the steps of:

receiving, in a receiving apparatus, an orthogonal frequency division multiplexing modulated signal having a changed bandwidth; and
changing a demodulation frequency bandwidth of said received signal to follow change of a frequency bandwidth of said modulated signal;
said changing step of said demodulation frequency bandwidth further including the steps of:
detecting a synchronizing signal from said received signal, comparing a phase of said detected synchronizing signal with a phase of a reference signal prepared on the basis of a current clock signal in said receiving apparatus, and changing a frequency of the clock signal in said receiving apparatus in accordance with a phase difference.

21. A receiving method according to Claim 20, wherein when an interval between adjacent carrier signals of said modulated signal is changed in accordance with change of a frequency of a clock signal in a transmission apparatus, omission of said carrier signals is detected when said received signal is decoded and said frequency of said clock signal in said receiving apparatus is controlled to dissolve the omission of said carrier signals.

22. An orthogonal frequency division multiplexing modulation communication apparatus comprising:

a transmission apparatus (1, 2T, 3A, 3B, 5, 8, 13T) for changing a setting of frequency bandwidth of a signal modulated in accordance with an orthogonal frequency division multiplexing modulation system and transmitting the modulated signal; and
a receiving apparatus (9, 4, 12, 3C, 2R, 7, 13R) for receiving said modulated signal and changing a demodu-

lation frequency bandwidth of the received signal to follow the change of said frequency bandwidth of said modulated signal.

23. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 22, comprising means (13T) for changing the number of carriers of said modulated signal to thereby change said frequency bandwidth.

24. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 23, wherein said transmission apparatus comprises a data rate conversion unit (1) for converting successively inputted data into data arrangement of frame unit constituted by a predetermined number of symbols, a coding unit (2T) for coding a signal supplied from said data rate conversion unit, an inverse Fourier transform unit (3A) for transforming the coded signal into a time-axis base signal, a synchronizing symbol insertion unit (5) for inserting a synchronizing symbol into the inverse Fourier transformed signal every predetermined symbol period, and an orthogonal modulation processing unit (8) for orthogonally modulating said synchronizing symbol inserted signal, said means (13T) for changing the number of carriers including means for changing an input data amount per unit time in said data rate conversion unit, changing an effective data period of said modulated signal in said coding unit, and changing a pattern of said synchronizing symbol added to the signal in said synchronizing symbol insertion unit.

25. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 24, wherein said receiving apparatus comprises an orthogonal demodulation processing unit (9) for orthogonally demodulating the received signal, a Fourier transform unit (3C) for transforming the demodulated signal into a frequency-axis base signal, a decoding unit (2R) for decoding the Fourier transformed signal, a data rate inverse-conversion unit (7) for converting the decoded signal into successive data, a synchronization detection unit (4) for detecting a synchronizing symbol from the received signal, and a control unit (13R), which changes a pattern of a reference signal for detection of said synchronizing symbol, changes an effective data period of the decoded signal in said decoding unit, and changes a taking-in period of data component in said data rate inverse-conversion unit in accordance with the change of the number of carriers in said transmission apparatus.

26. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 24, wherein said receiving apparatus comprises an orthogonal demodulation processing unit (9) for orthogonally demodulating the received signal, a Fourier transform unit (3C) for transforming the demodulated signal into a frequency-axis base signal, a decoding unit (2R) for decoding the Fourier transformed signal, a data rate inverse-conversion unit (7) for converting the decoded signal into successive data, a synchronization detection unit (15) for detecting a synchronizing symbol from the received signal, a data confirmation unit (18) for detecting the number of carrier signals from the Fourier transformed signal, and a control unit (13RC), which produces a control signal for changing a pattern of a reference signal for detection of said synchronizing symbol, changing an effective data period of the decoded signal in said decoding unit, and changing a taking-in period of data component in said data rate inverse-conversion unit when said data confirmation unit detects that the number of carriers is changed.

27. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 25 or 26, wherein said transmission apparatus further comprises transmission level changing means (82) for adjusting a level of the transmission signal in accordance with the change of the number of carriers and changing a gain of said coding unit or said inverse Fourier transform unit by an inverse number of a value multiplied by a square root of a change rate of the number of carriers and said receiving apparatus further comprises reception level changing means for adjusting a level of the received signal in accordance with the change of the number of carriers and for changing a gain of said Fourier transform unit or said decoding unit by an inverse number of a value multiplied by a square root of the change rate of the number of carriers.

28. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 22, wherein the change of the number of carriers is made every symbols of said modulated signal.

29. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 22, further comprising a monitoring apparatus (106) for monitoring a state of a communication path and producing a control signal for changing the frequency bandwidth of the signal to be transmitted and wherein said transmission apparatus changes the frequency bandwidth of the signal modulated by the orthogonal frequency division multiplexing modulation system in accordance with said control signal.

30. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 22, com-

prising means for changing the frequency bandwidth by changing a frequency of a clock signal used in said transmission apparatus.

31. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 30, wherein said transmission apparatus comprises a data rate conversion unit (1) for converting successively inputted data into data arrangement of frame unit constituted by a predetermined number of symbols, a coding unit (2T) for coding a signal supplied from said data rate conversion unit, an inverse Fourier transform unit (3A) for transforming the coded signal into a time-axis base signal, a synchronizing symbol insertion unit (5) for inserting a synchronizing symbol into the inverse Fourier transformed signal every predetermined symbol period, and an orthogonal modulation processing unit (8) for orthogonally modulating said synchronizing symbol inserted signal, and said means for changing the frequency bandwidth includes said data rate conversion unit, said coding unit, said inverse Fourier conversion unit, said synchronizing symbol insertion unit, and means (11) for changing the frequency of the clock signal supplied to said orthogonal modulation processing unit.

32. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 31, wherein said receiving apparatus comprises an orthogonal demodulation processing unit (9) for orthogonally demodulating the received signal, a Fourier transform unit (3C) for transforming the demodulated signal into a frequency-axis base signal, a decoding unit (2R) for decoding the Fourier transformed signal, a data rate inverse-conversion unit (7) for converting the decoded signal into successive data, a synchronization detection unit (4) for detecting a synchronizing symbol from the received signal, a data confirmation unit for detecting change of the frequency bandwidth of the modulated signal on the basis of the decoded signal, a clock signal generation unit for supplying a clock signal to said orthogonal demodulation processing unit, said Fourier transform unit, said decoding unit, said data rate conversion unit, said synchronization detection unit and said data confirmation unit, and means for changing a frequency of the clock signal of said clock signal generation unit in accordance with detection of the change of the frequency bandwidth.

33. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 32, wherein said receiving apparatus comprises a clock rate conversion unit for detecting said synchronizing symbol from the received signal and comparing a phase of said detected synchronizing symbol with a phase of a reference signal prepared on the basis of a current clock signal in said clock signal generation unit so that the frequency of the clock signal in said receiving apparatus is changed in accordance with a phase difference.

34. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 32, wherein an interval between adjacent carrier signals of said modulated signal is changed by changing of the frequency of the clock signal in said transmission apparatus and omission of said carrier signals in the decoded signal in said decoding unit of said receiving apparatus is detected, so that said changing means of said clock signal frequency controls the frequency of said clock signal generation unit so that omission of said carrier signals is dissolved.

35. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 34, wherein said clock signal generation unit of said receiving apparatus includes a clock signal generator for changing the frequency by a first change amount and a second clock signal changing unit for further changing the clock frequency by a second change amount.

36. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 22, further comprising a monitoring apparatus (106) for monitoring a state of a communication path and producing a control signal for changing the frequency bandwidth of the signal to be transmitted and wherein said transmission apparatus changes the frequency bandwidth of the signal modulated by the orthogonal frequency division multiplexing modulation system in accordance with said control signal from said monitoring apparatus.

37. An orthogonal frequency division multiplexing modulation communication apparatus according to Claim 22, wherein said orthogonal frequency division multiplexing modulation system is a digital modulation system for at least one wave of carriers being a quadrature amplitude modulation system.

38. A transmission apparatus for an orthogonal frequency division multiplexing modulated signal, comprising:

a data rate conversion unit (1) for converting successively inputted data into data arrangement of frame unit constituted by a predetermined number of symbols;

a coding unit (2T) for coding a signal supplied from said data rate conversion unit;
an inverse Fourier transform unit (3A) for transforming the coded signal into a time-axis base signal;
a synchronizing symbol insertion unit (5) for inserting a synchronizing symbol into the inverse Fourier transformed signal every predetermined symbol period;
an orthogonal modulation processing unit (8) for orthogonally modulating said synchronizing symbol inserted signal; and
means (13T) for changing an input data amount per unit time in said data rate conversion unit, changing an effective data period of said modulated signal in said coding unit, and changing a pattern of said synchronizing symbol added to the signal in said synchronizing symbol insertion unit to thereby control the number of carriers of a transmission signal to change a frequency bandwidth of the transmission signal.

39. A transmission apparatus for an orthogonal frequency division multiplexing modulated signal, comprising:

a data rate conversion unit (1) for converting successively inputted data into data arrangement of frame unit constituted by a predetermined number of symbols;
a coding unit (2T) for coding a signal supplied from said data rate conversion unit;
an inverse Fourier transform unit (3A) for transforming the coded signal into a time-axis base signal;
a synchronizing symbol insertion unit (5) for inserting a synchronizing symbol into the inverse Fourier transformed signal every predetermined symbol period;
an orthogonal modulation processing unit (8) for orthogonally modulating said synchronizing symbol inserted signal; and
means for changing a frequency bandwidth in accordance with change of a frequency of a clock signal used in said transmission apparatus and including said data rate conversion unit, said coding unit, said inverse Fourier transform unit, said synchronizing symbol insertion unit and means for changing a frequency of a clock signal supplied to said orthogonal modulation processing unit.

40. A receiving apparatus for an orthogonal frequency division multiplexing modulated signal, comprising:

an orthogonal demodulation processing unit (9) for receiving the orthogonal frequency division multi-plexing modulated signal having a bandwidth changed by changing the number of carriers and orthogonally demodulating the received signal;
a Fourier transform unit (3C) for transforming the demodulated signal into a frequency-axis base signal;
a decoding unit (2R) for decoding the Fourier transformed signal;
a data rate inverse-conversion unit (7) for converting the decoded signal into successive data;
a synchronization detection unit (4) for detecting a synchronizing symbol from the received signal; and
a control unit (13R) for changing a pattern of a reference signal for detection of said synchronizing symbol, changing an effective data period of the decoded signal in said decoding unit, and changing a taking-in period of data component in said data rate inverse-conversion unit in accordance with the change of the number of carriers.

41. A receiving apparatus for an orthogonal frequency division multiplexing modulated signal, comprising:

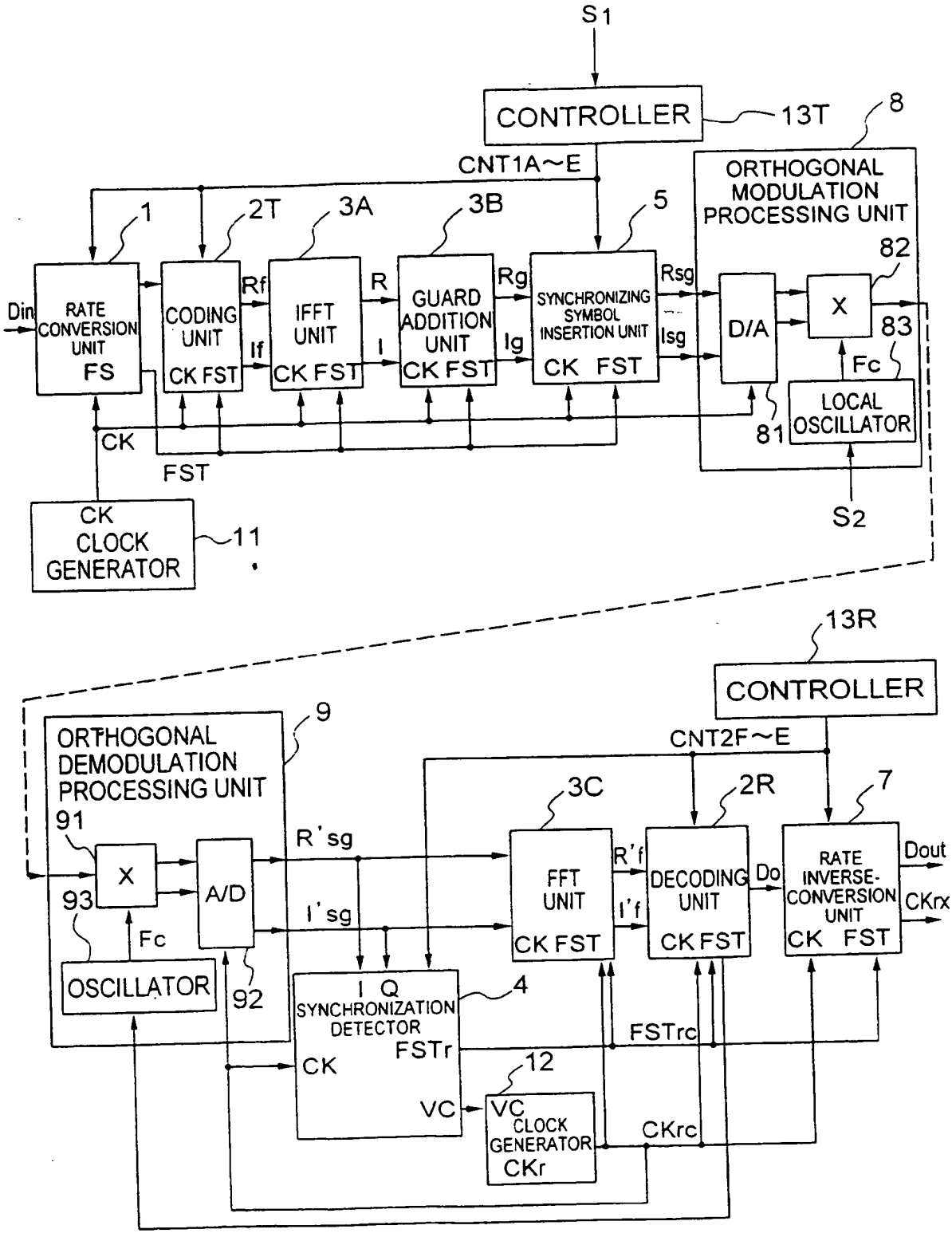
an orthogonal demodulation processing unit (9) for receiving the orthogonal frequency division multiplexing modulated signal having a bandwidth changed by changing the number of carriers and orthogonally demodulating the received signal;
a Fourier transform unit (3C) for transforming the demodulated signal into a frequency-axis base signal;
a decoding unit (2R) for decoding the Fourier transformed signal;
a data rate inverse-conversion unit (7) for converting the decoded signal into successive data;
a synchronization detection unit (4) for detecting a synchronizing symbol from the received signal;
a data confirmation unit for detecting the number of carrier signals from the Fourier transformed signal; and
a control unit (13R) for producing a control signal for changing a pattern of a reference signal for detection of said synchronizing symbol, changing an effective data period of the decoded signal in said decoding unit, and changing a taking-in period of data component in said data rate inverse-conversion unit when said data confirmation unit detects that the number of carriers is changed.

42. A receiving apparatus for an orthogonal frequency division multiplexing modulated signal, comprising:

an orthogonal demodulation processing unit (9) for receiving the orthogonal frequency division multiplexing

modulated signal having a changed bandwidth and orthogonally demodulating the received signal;
a Fourier transform unit (3C) for transforming the demodulated signal into a frequency-axis base signal;
a decoding unit (2R) for decoding the Fourier transformed signal;
a data rate inverse-conversion unit (7) for converting the decoded signal into successive data;
a synchronization detection unit (4) for detecting a synchronizing symbol from the received signal;
a data confirmation unit for detecting change of a frequency bandwidth of said modulated signal on the basis of the decoded signal;
a clock signal generating unit for supplying a clock signal to said orthogonal demodulation processing unit, said Fourier transform unit, said coding unit, said data rate conversion unit, said synchronization detection unit and said data confirmation unit; and
means for changing a frequency of the clock signal of said clock signal generation unit in accordance with detection of the change of the frequency bandwidth.

FIG. 1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13T
8
CNT1A~E
ORTHOGONAL MODULATION PROCESSING UNIT
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2T
3A
3B
5
82
Din
RATE CONVERSION UNIT
FS
CODING UNIT
CK FST
Rf
If
IFFT UNIT
CK FST
R
I
GUARD ADDITION UNIT
CK FST
Rg
Ig
SYNCHRONIZING SYMBOL INSERTION UNIT
CK FST
Rsg
Isg
D/A
X
83
Fc
LOCAL OSCILLATOR
81
CK
FST
CK CLOCK GENERATOR
11
S2
13R
CONTROLLER
9
ORTHOGONAL DEMODULATION PROCESSING UNIT
CNT2F~E
3C
2R
7
91
X
A/D
R'sg
I'sg
93
Fc
OSCILLATOR
92
FFT UNIT
CK FST
R'f
I'f
DECODING UNIT
CK FST
Do
RATE INVERSE-CONVERSION UNIT
CK FST
Dout
CKrx
I Q SYNCHRONIZATION DETECTOR
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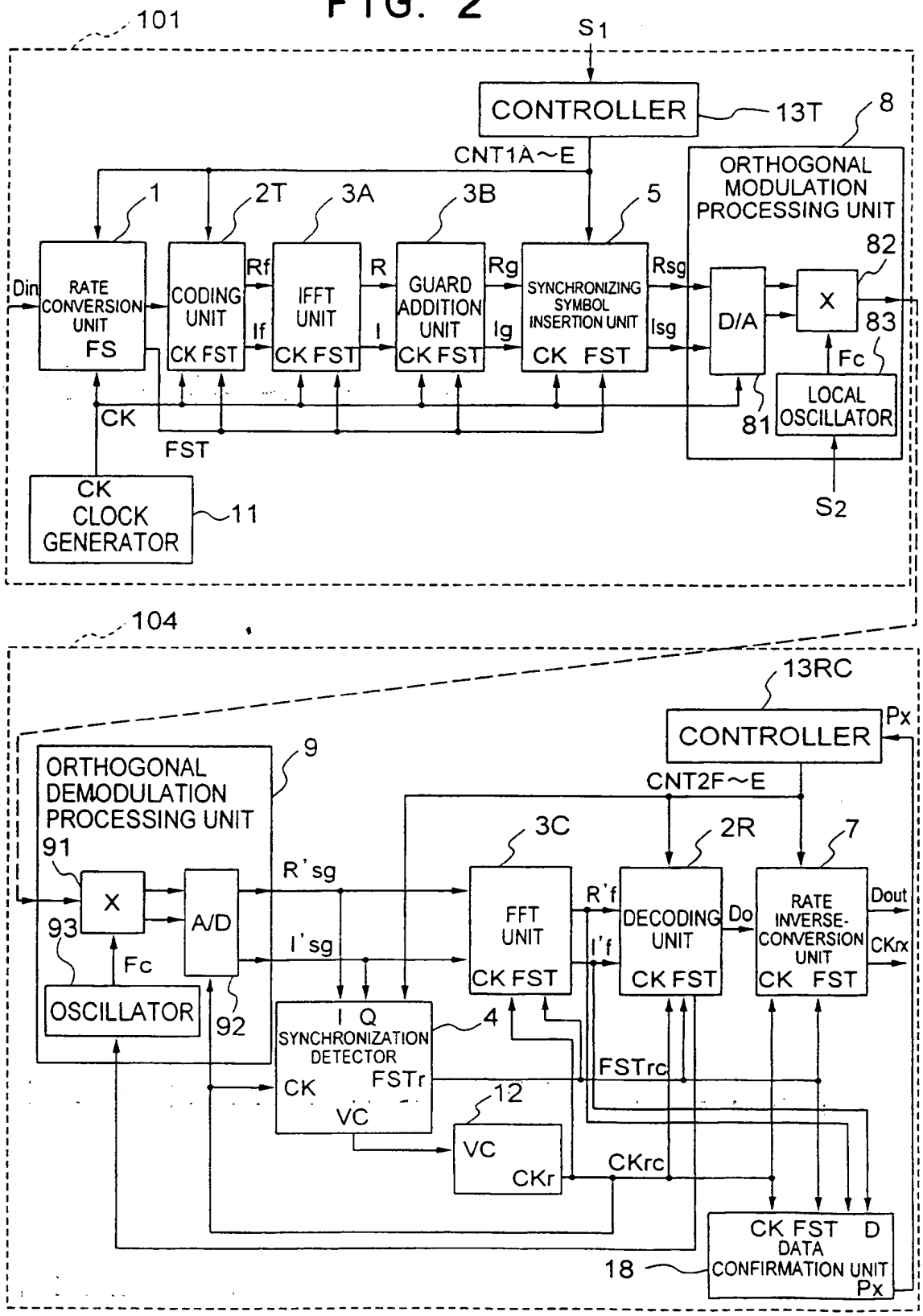
FSTr
FSTrc
12
VC
VC CLOCK GENERATOR
CKr
CKrc

FIG. 2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S1
CONTROLLER
13T
8
CNT1A~E
ORTHOGONAL MODULATION PROCESSING UNIT
1
2T
3A
3B
5
82
Din
RATE CONVERSION UNIT
FS
CODING UNIT
CK FST
Rf
If
IFFT UNIT
CK FST
R
I
GUARD ADDITION UNIT
CK FST
Rg
Ig
SYNCHRONIZING SYMBOL INSERTION UNIT
CK FST
Rsg
Isg
D/A
X
83
Fc
LOCAL OSCILLATOR
81
CK
FST
CK CLOCK GENERATOR
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S2
104
13RC
CONTROLLER
Px
CNT2F~E
ORTHOGONAL DEMODULATION PROCESSING UNIT
9
91
3C
2R
7
X
93
A/D
R'sg
I'sg
FFT UNIT
CK FST
R'f
I'f
DECODING UNIT
CK FST
Do
RATE INVERSE-CONVERSION UNIT
CK FST
Dout
CKrx
Fc
OSCILLATOR
92
I Q SYNCHRONIZATION DETECTOR
CK
FSTr
VC
4
FSTrc
12
VC
CKr
CKrc
CK FST D
DATA CONFIRMATION UNIT
Px
18

FIG. 3

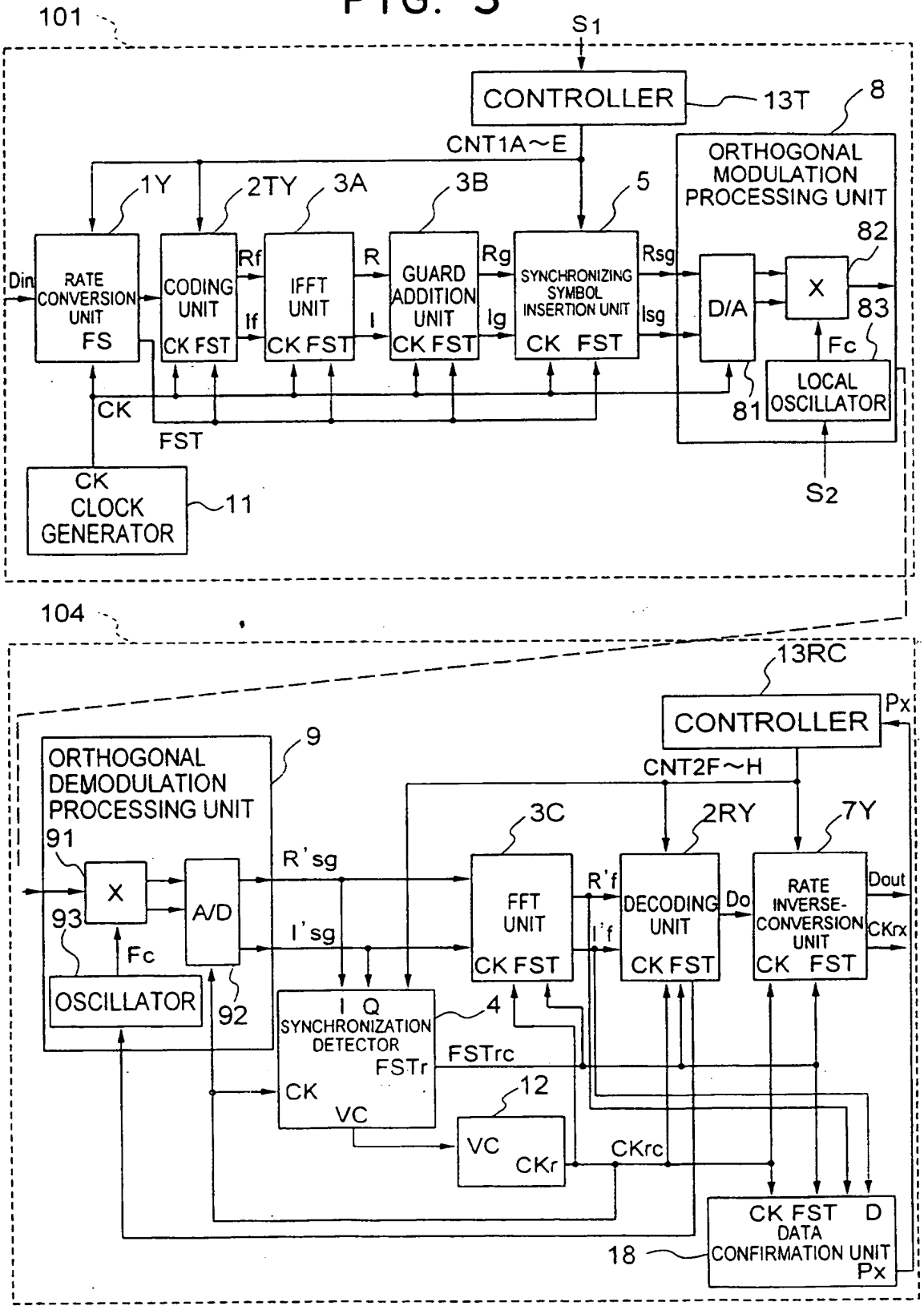

101
S1
CONTROLLER
13T
8
CNT1A~E
ORTHOGONAL MODULATION PROCESSING UNIT
1Y
2TY
3A
3B
5
82
Din
RATE CONVERSION UNIT
FS
CODING UNIT
CK FST
Rf
If
IFFT UNIT
CK FST
R
I
GUARD ADDITION UNIT
CK FST
Rg
Ig
SYNCHRONIZING SYMBOL INSERTION UNIT
CK FST
Rsg
Isg
D/A
X
83
Fc
LOCAL OSCILLATOR
81
CK
FST
CK CLOCK GENERATOR
11
S2
104
13RC
CONTROLLER
Px
CNT2F~H
ORTHOGONAL DEMODULATION PROCESSING UNIT
9
91
3C
2RY
7Y
R'sg
I'sg
X
A/D
93
Fc
OSCILLATOR
92
FFT UNIT
CK FST
R'f
I'f
DECODING UNIT
CK FST
Do
RATE INVERSE-CONVERSION UNIT
CK FST
Dout
CKrx
I Q SYNCHRONIZATION DETECTOR
FSTr
4
FSTrc
CK
VC
12
VC
CKr
CKrc
CK FST D
DATA CONFIRMATION UNIT
Px
18

FIG. 4

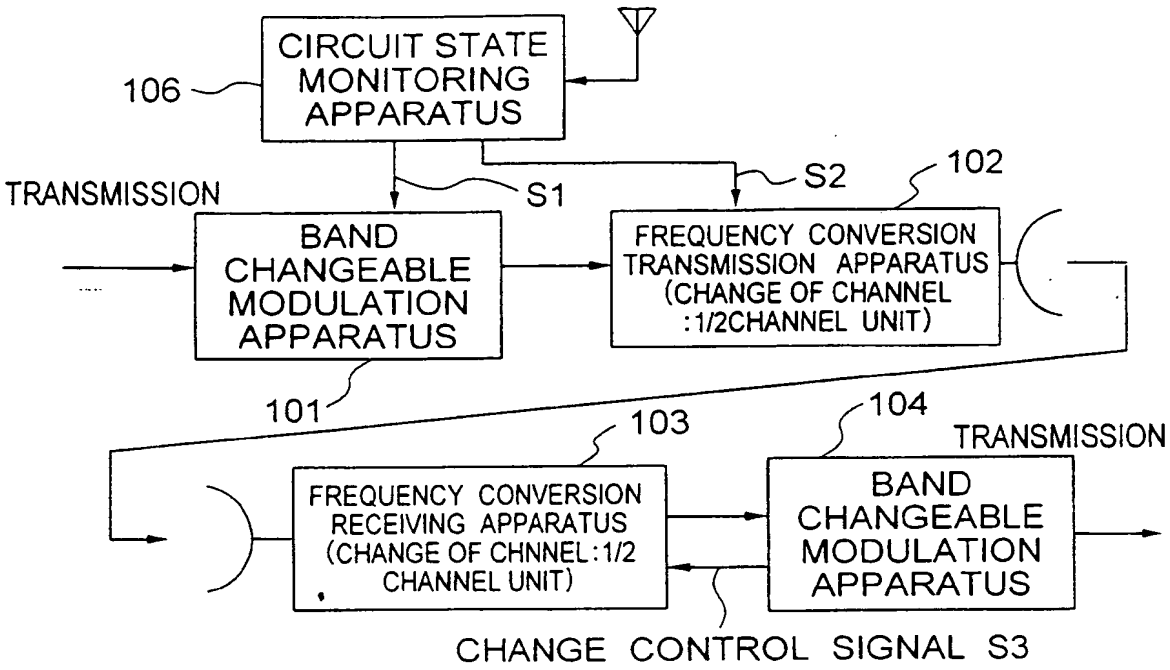

CIRCUIT STATE MONITORING APPARATUS
106
TRANSMISSION
S1
S2
102
BAND CHANGEABLE MODULATION APPARATUS
FREQUENCY CONVERSION TRANSMISSION APPARATUS (CHANGE OF CHANNEL :1/2CHANNEL UNIT)
101
103
104
TRANSMISSION
FREQUENCY CONVERSION RECEIVING APPARATUS (CHANGE OF CHNNEL:1/2 CHANNEL UNIT)
BAND CHANGEABLE MODULATION APPARATUS
CHANGE CONTROL SIGNAL S3

FIG. 5

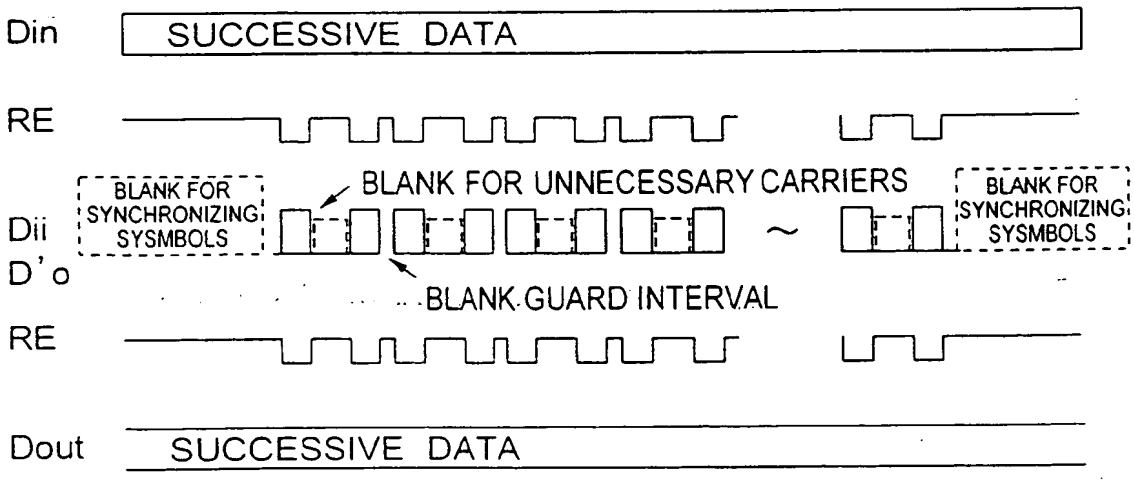

Din
SUCCESSIVE DATA
RE
BLANK FOR SYNCHRONIZING SYSMBOLS
BLANK FOR UNNECESSARY CARRIERS
BLANK FOR SYNCHRONIZING SYSMBOLS
Dii
D'o
BLANK GUARD INTERVAL
RE
Dout
SUCCESSIVE DATA

FIG. 6

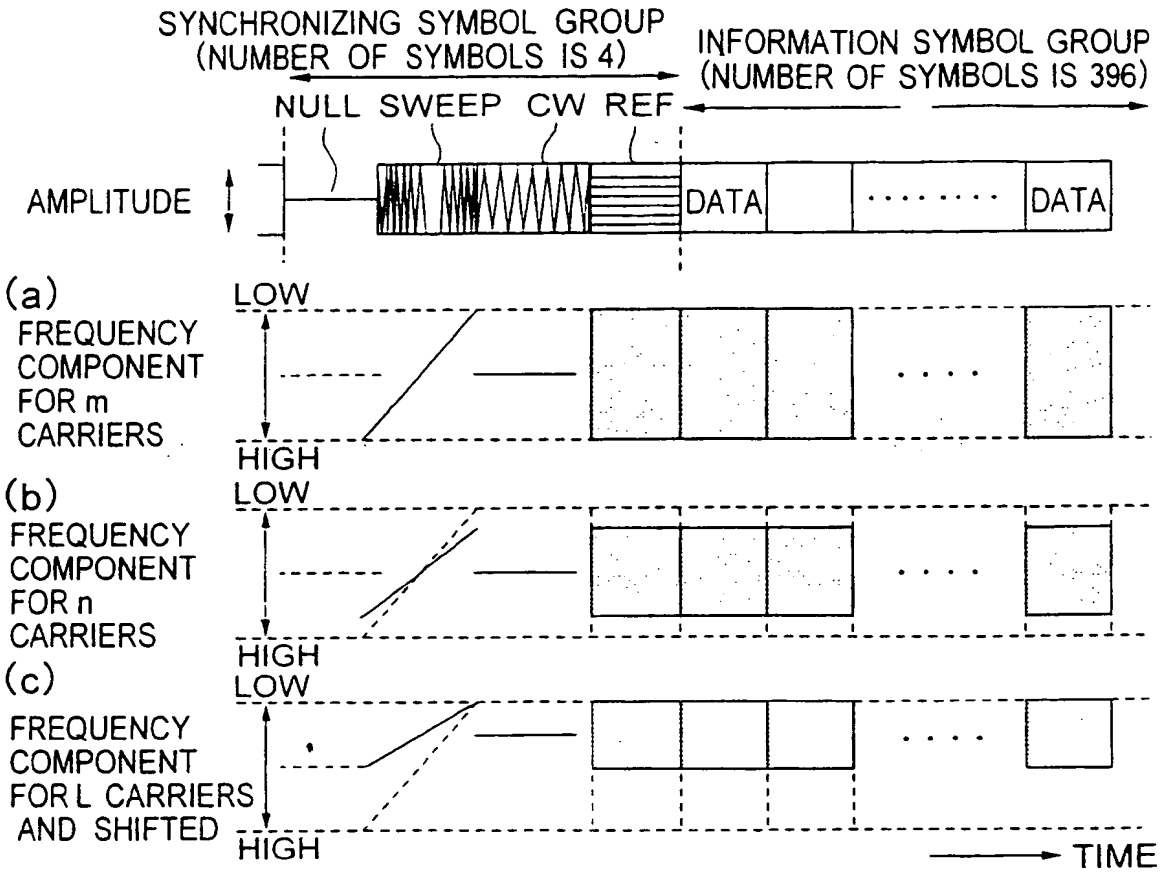

SYNCHRONIZING SYMBOL GROUP
(NUMBER OF SYMBOLS IS 4)
INFORMATION SYMBOL GROUP
(NUMBER OF SYMBOLS IS 396)
NULL
SWEEP
CW
REF
AMPLITUDE
DATA
DATA
(a)
FREQUENCY COMPONENT FOR m CARRIERS
LOW
HIGH
(b)
FREQUENCY COMPONENT FOR n CARRIERS
LOW
HIGH
(c)
FREQUENCY COMPONENT FOR L CARRIERS AND SHIFTED
LOW
HIGH
TIME

FIG. 7

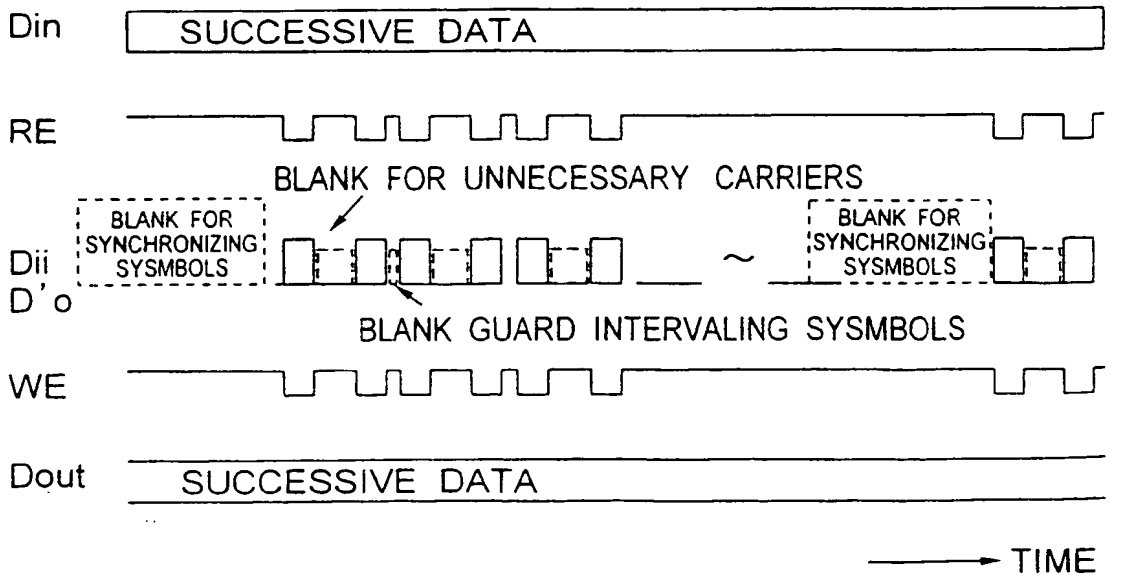
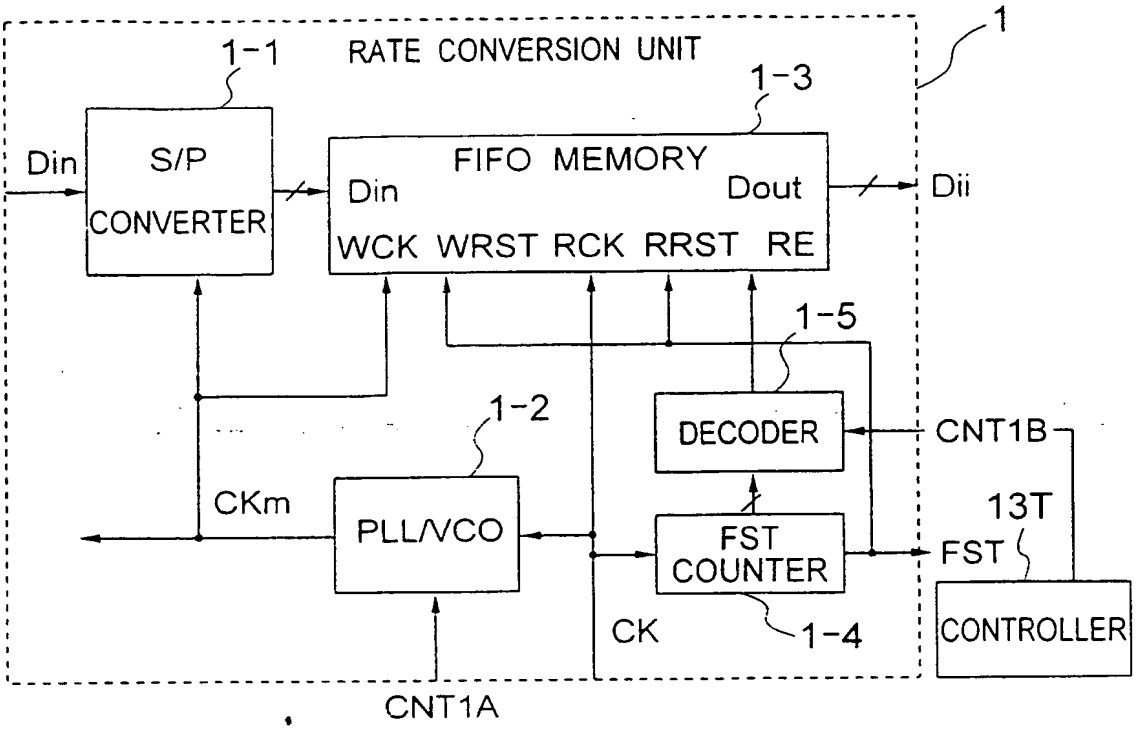

Din
SUCCESSIVE DATA
RE
BLANK FOR UNNECESSARY CARRIERS
BLANK FOR SYNCHRONIZING SYSMBOLS
BLANK FOR SYNCHRONIZING SYSMBOLS
Dii
D'o
BLANK GUARD INTERVALING SYSMBOLS
WE
Dout
SUCCESSIVE DATA
TIME

FIG. 8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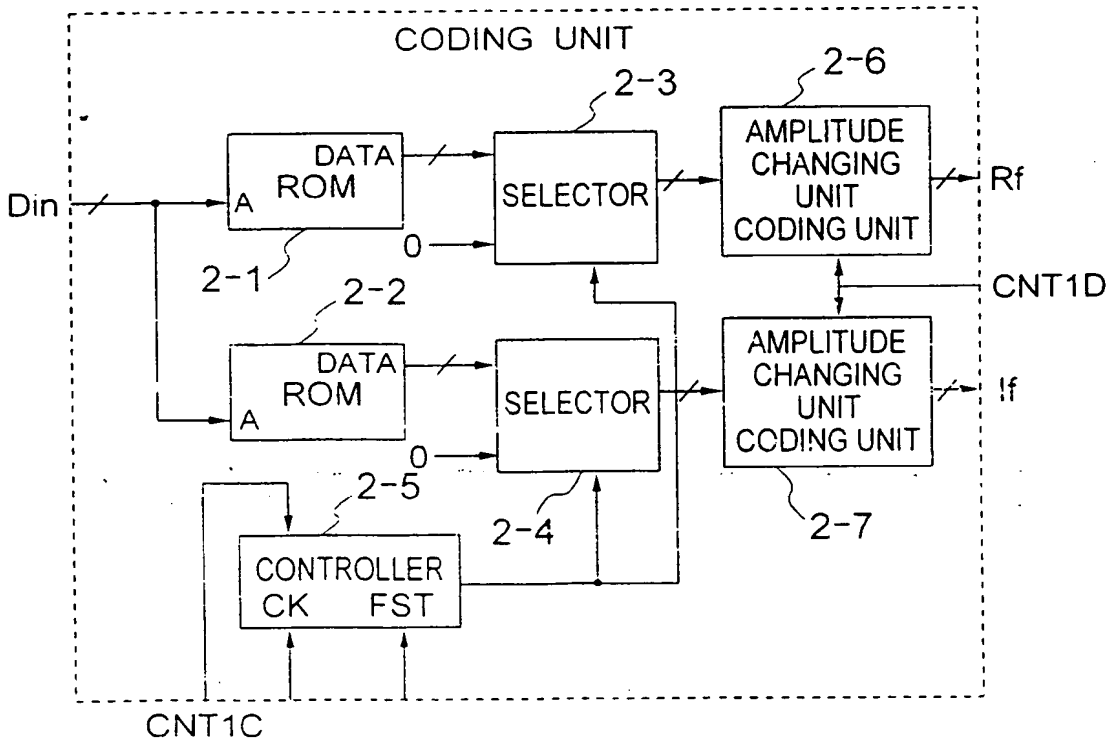
1-1
1-3
Din
S/P
CONVERTER
FIFO MEMORY
Din
Dout
Dii
WCK WRST RCK RRST RE
1-5
1-2
DECODER
CNT1B
CKm
PLL/VCO
13T
FST
COUNTER
FST
CONTROLLER
CK
1-4
CNT1A

FIG. 9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2-3
AMPLITUDE
CHANGING
UNIT
CODING UNIT
Rf
Din
DATA
ROM
A
SELECTOR
0
2-1
CNT1D
2-2
DATA
ROM
A
SELECTOR
AMPLITUDE
CHANGING
UNIT
CODING UNIT
If
0
2-5
2-4
2-7
CONTROLLER
CK FST
CNT1C

FIG. 10

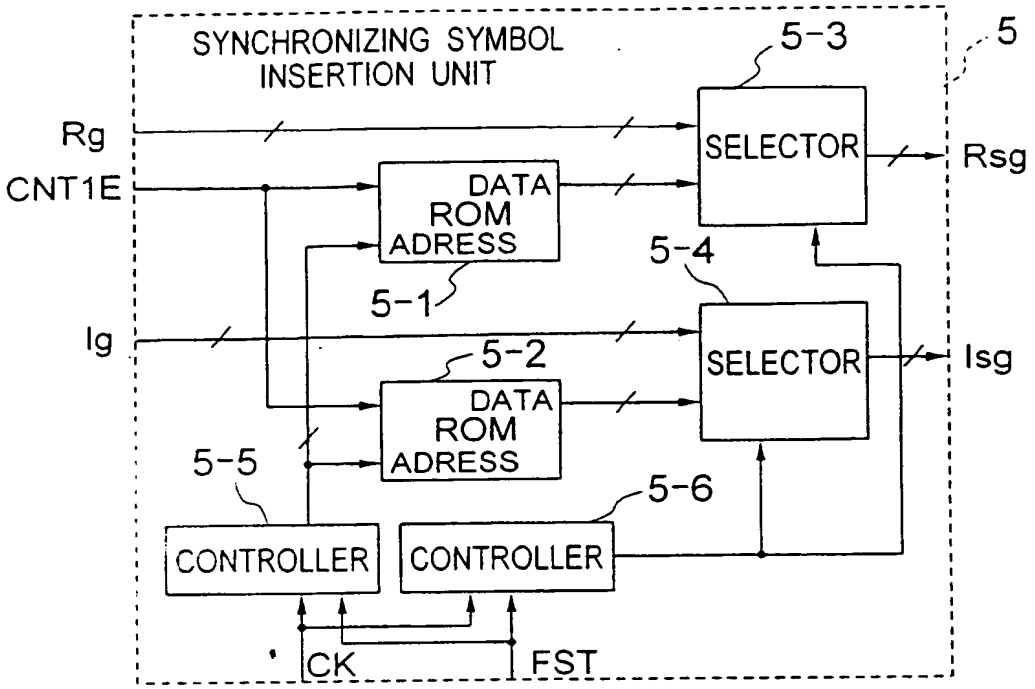

SYNCHRONIZING SYMBOL INSERTION UNIT
5
5-3
SELECTOR
Rg
Rsg
CNT1E
DATA ROM ADRESS
5-1
5-4
SELECTOR
Ig
Isg
5-2
DATA ROM ADRESS
5-5
5-6
CONTROLLER
CONTROLLER
CK
FST

FIG. 11

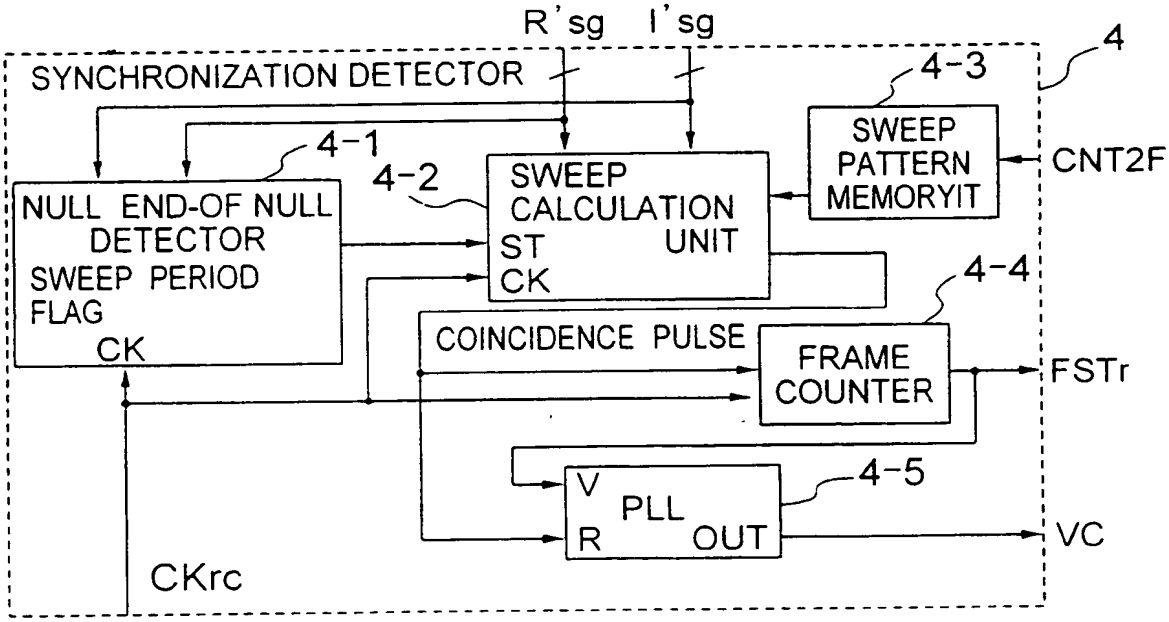

R'sg
I'sg
SYNCHRONIZATION DETECTOR
4
4-3
SWEEP PATTERN MEMORYIT
CNT2F
4-1
4-2
NULL END-OF NULL DETECTOR
SWEEP PERIOD FLAG
CK
SWEEP CALCULATION UNIT
ST
CK
4-4
COINCIDENCE PULSE
FRAME COUNTER
FSTr
V
R
PLL
OUT
4-5
VC
CKrc

FIG. 12

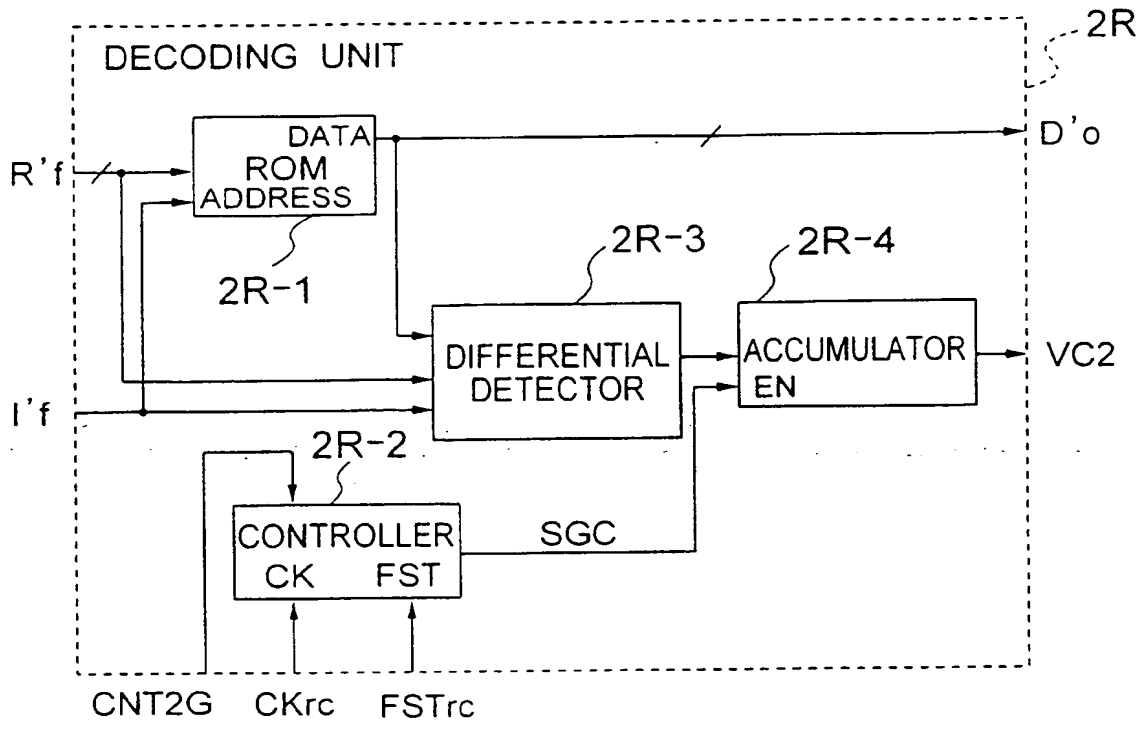

DECODING UNIT
2R
DATA
ROM
ADDRESS
R'f
D'o
2R-1
2R-3
2R-4
DIFFERENTIAL
DETECTOR
ACCUMULATOR
EN
VC2
I'f
2R-2
CONTROLLER
CK FST
SGC
CNT2G
CKrc
FSTrc

FIG. 13

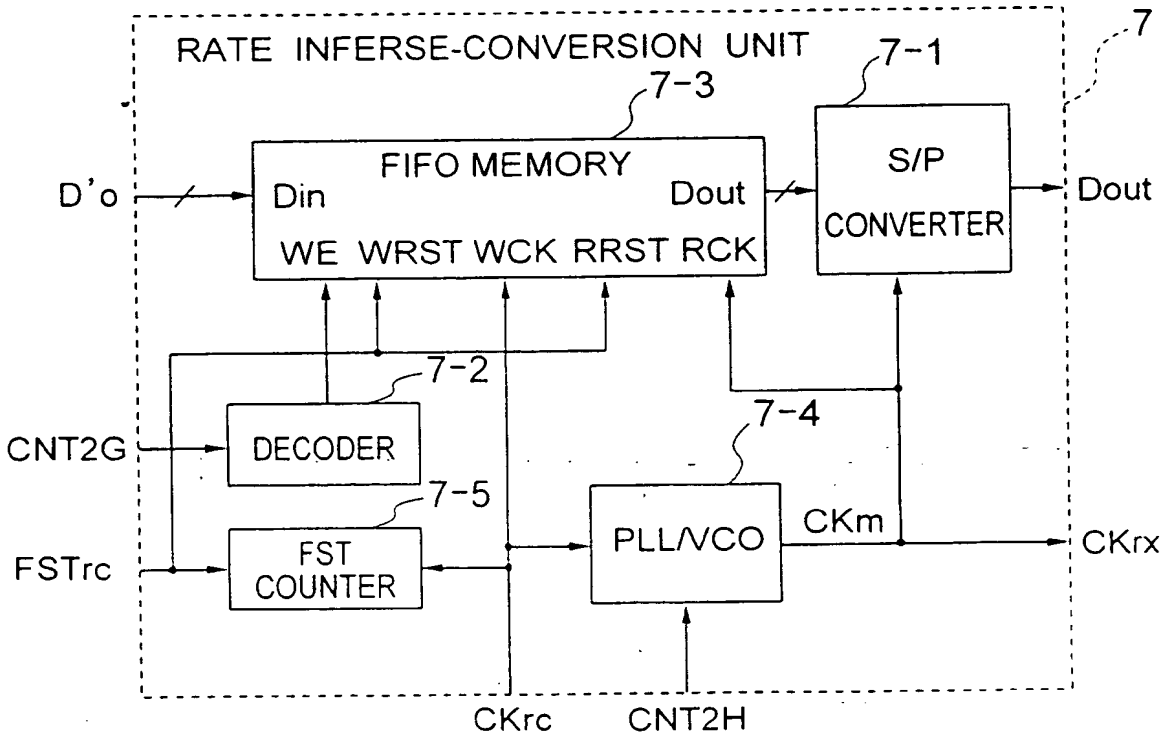

RATE INFERSE-CONVERSION UNIT
7
7-1
7-3
FIFO MEMORY
Din
Dout
WE WRST WCK RRST RCK
S/P
CONVERTER
D'o
Dout
7-2
7-4
CNT2G
DECODER
7-5
CKm
FSTrc
FST
COUNTER
PLL/VCO
CKrx
CKrc
CNT2H

FIG. 14

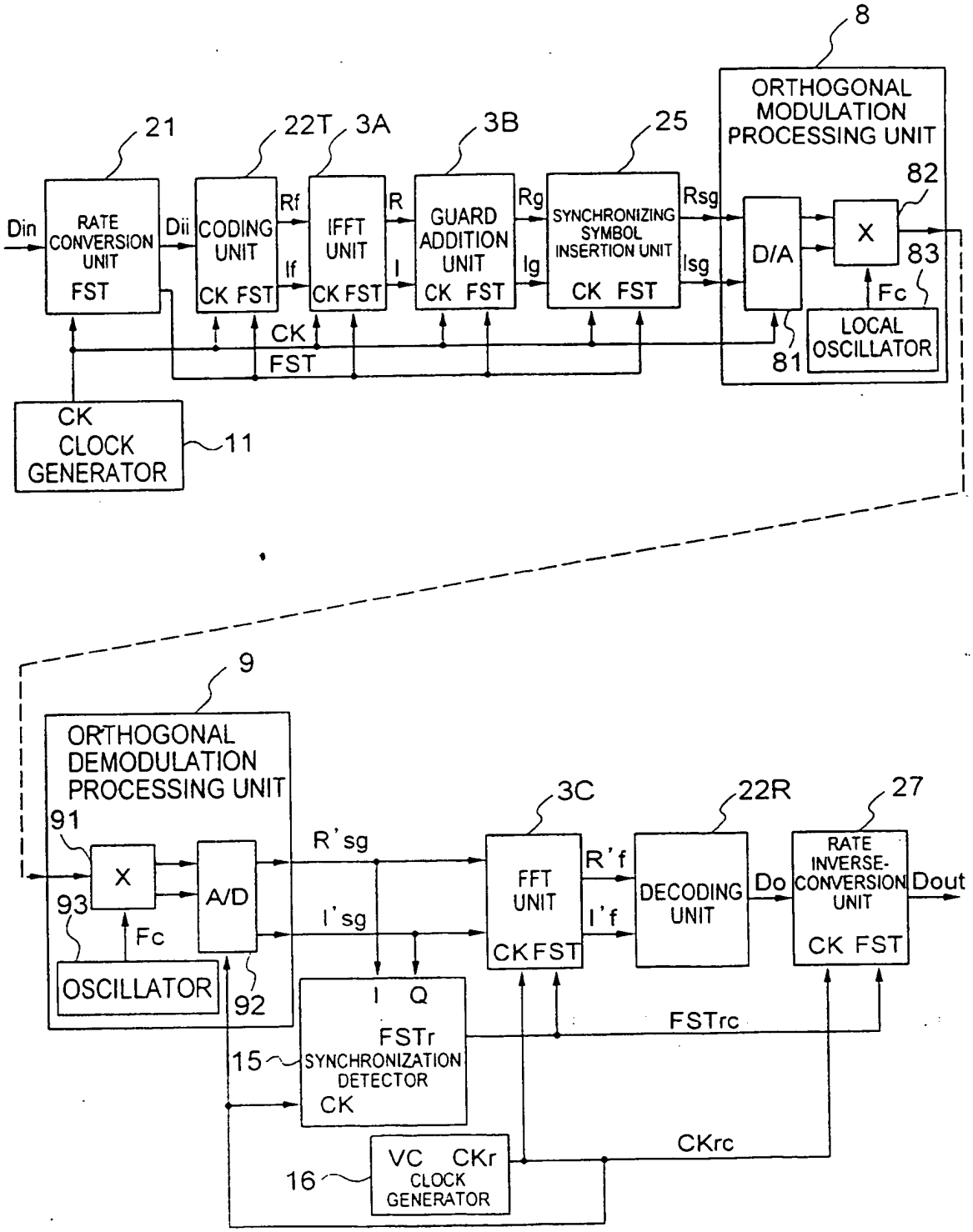

8
ORTHOGONAL MODULATION PROCESSING UNIT
21
22T
3A
3B
25
Din
RATE CONVERSION UNIT
FST
Dii
CODING UNIT
CK FST
Rf
If
IFFT UNIT
CK FST
R
I
GUARD ADDITION UNIT
CK FST
Rg
Ig
SYNCHRONIZING SYMBOL INSERTION UNIT
CK FST
Rsg
Isg
D/A
X
82
83
Fc
LOCAL OSCILLATOR
81
CK
FST
CK CLOCK GENERATOR
11
9
ORTHOGONAL DEMODULATION PROCESSING UNIT
91
X
93
Fc
A/D
92
OSCILLATOR
R'sg
I'sg
3C
FFT UNIT
CK FST
R'f
I'f
22R
DECODING UNIT
Do
27
RATE INVERSE-CONVERSION UNIT
CK FST
Dout
I Q
FSTr
15
SYNCHRONIZATION DETECTOR
CK
FSTrc
CKrc
16
VC CKr
CLOCK GENERATOR

FIG. 15A

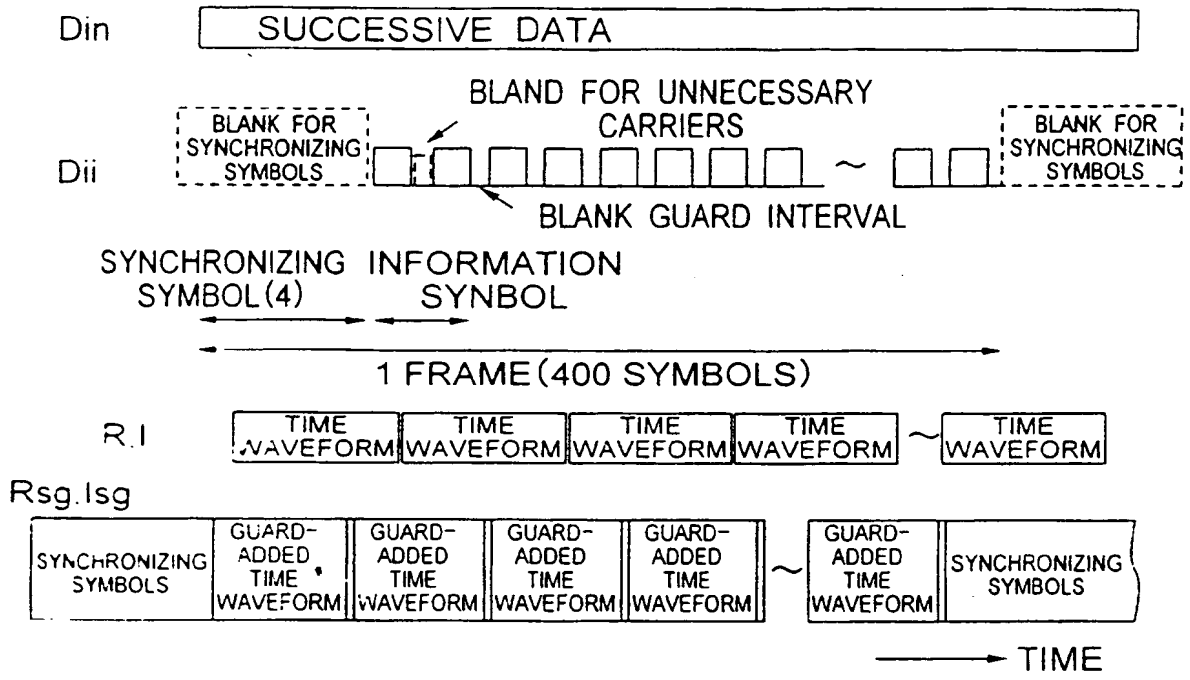


FIG. 15B

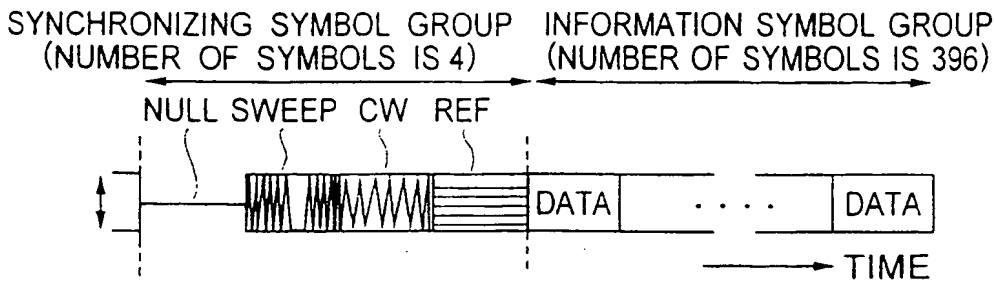


FIG. 16

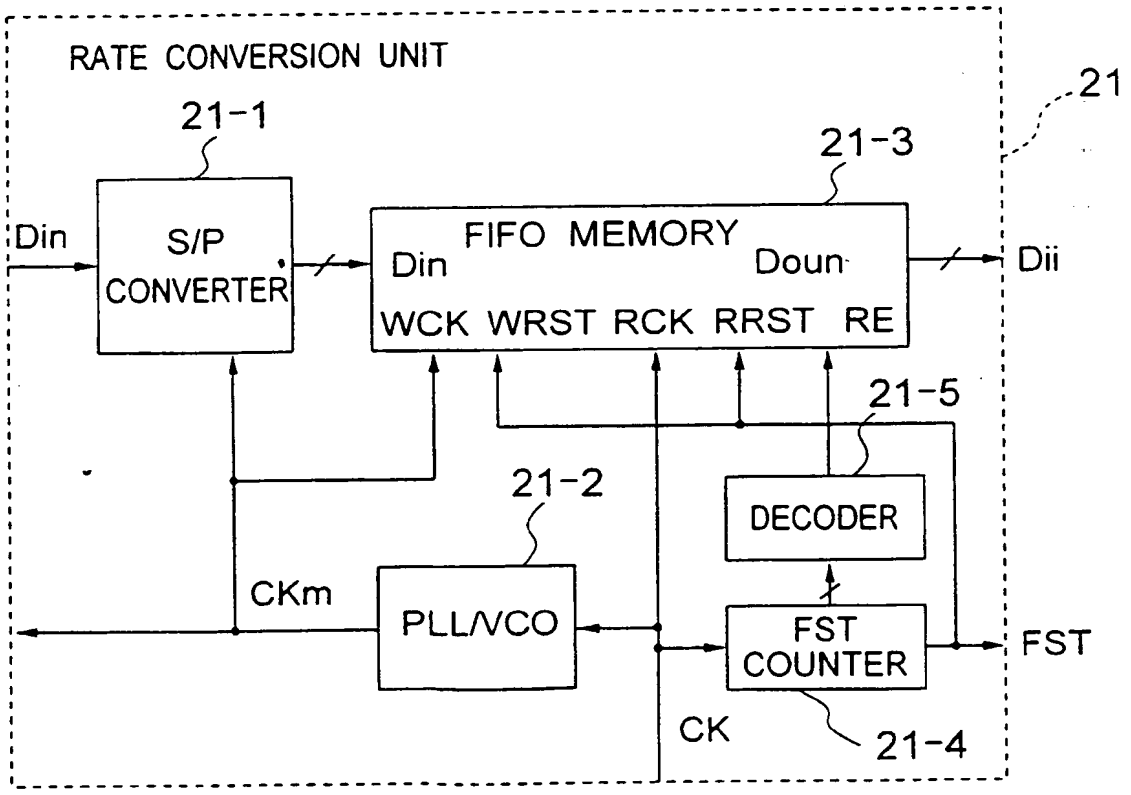

RATE CONVERSION UNIT
21
21-1
21-3
Din
S/P
CONVERTER
FIFO MEMORY
Din
Doun
WCK WRST RCK RRST RE
Dii
21-5
21-2
DECODER
CKm
PLL/VCO
FST
COUNTER
FST
CK
21-4

FIG. 17

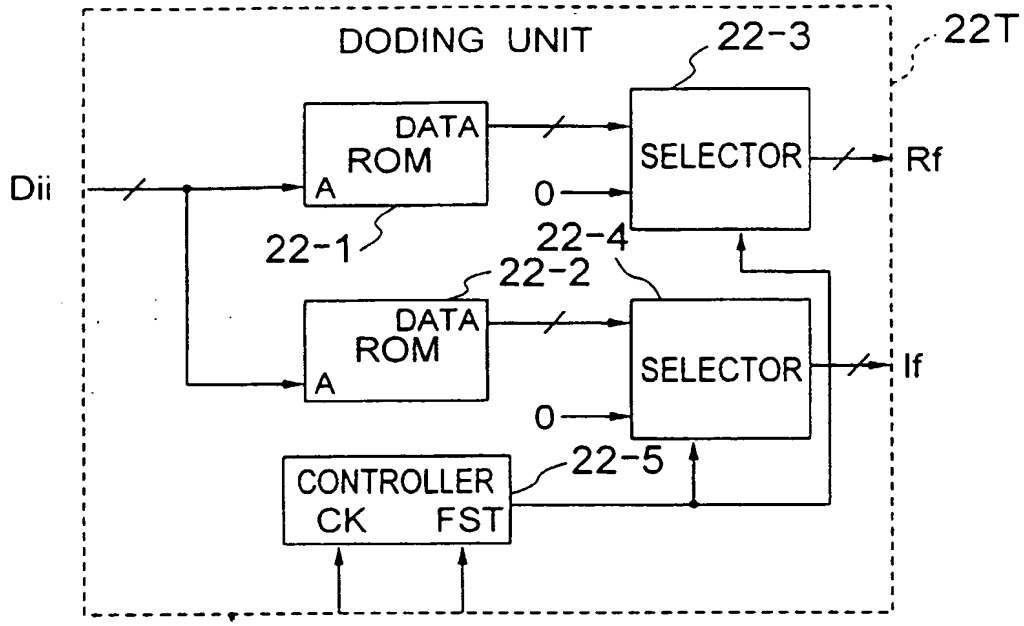

DODING UNIT
22T
22-3
DATA
ROM
A
SELECTOR
Rf
Dii
0
22-1
22-4
22-2
DATA
ROM
A
SELECTOR
If
0
22-5
CONTROLLER
CK
FST

FIG. 18

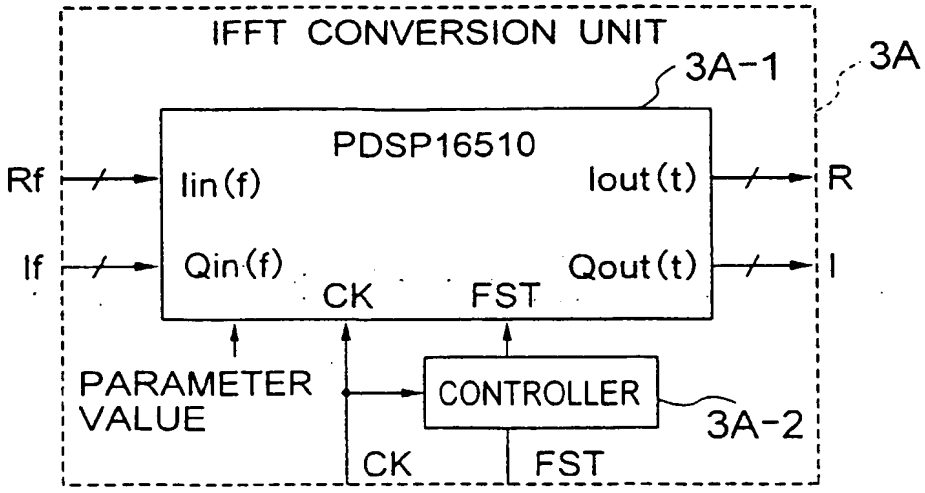

IFFT CONVERSION UNIT
3A-1
3A
PDSP16510
Rf
Iin(f)
Iout(t)
R
If
Qin(f)
Qout(t)
I
CK
FST
PARAMETER
VALUE
CONTROLLER
3A-2
CK
FST

FIG. 19

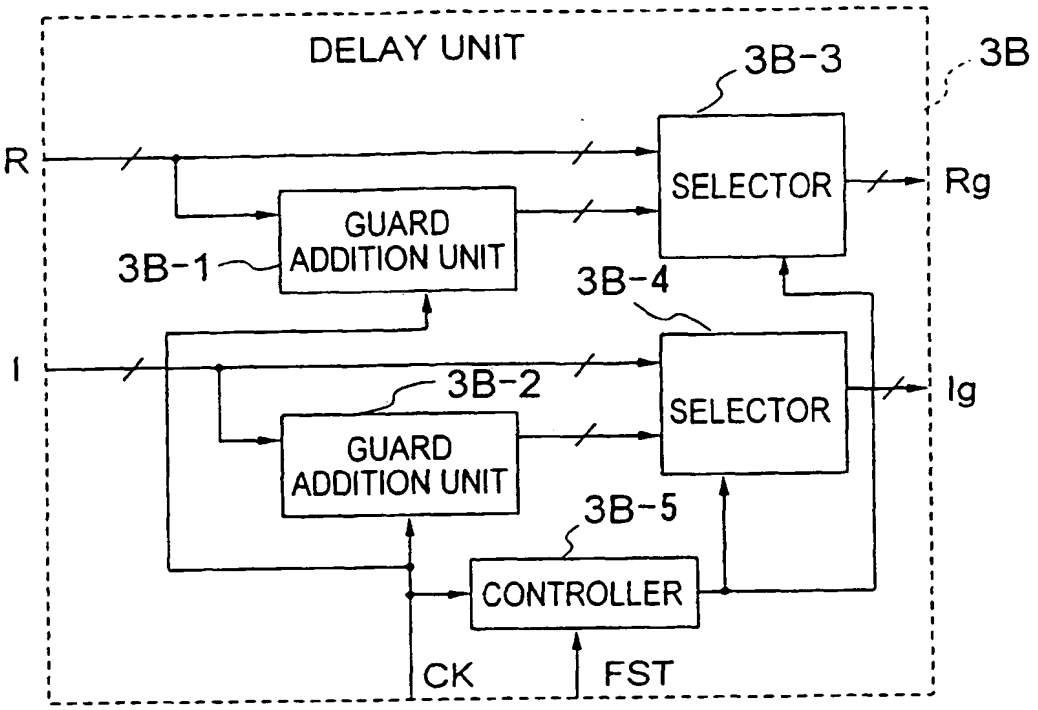

DELAY UNIT
3B
3B-3
R
SELECTOR
Rg
GUARD ADDITION UNIT
3B-1
3B-4
I
SELECTOR
Ig
3B-2
GUARD ADDITION UNIT
3B-5
CONTROLLER
CK
FST

FIG. 20

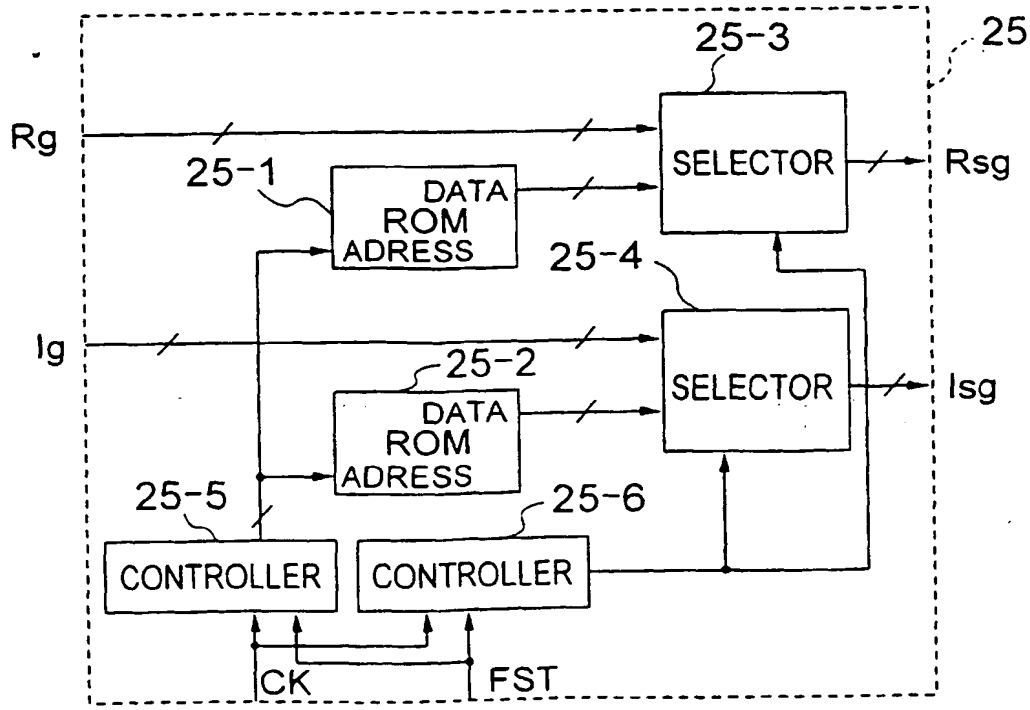

25
25-3
Rg
SELECTOR
Rsg
25-1
DATA ROM ADRESS
25-4
Ig
SELECTOR
Isg
25-2
DATA ROM ADRESS
25-5
25-6
CONTROLLER
CONTROLLER
CK
FST

FIG. 21

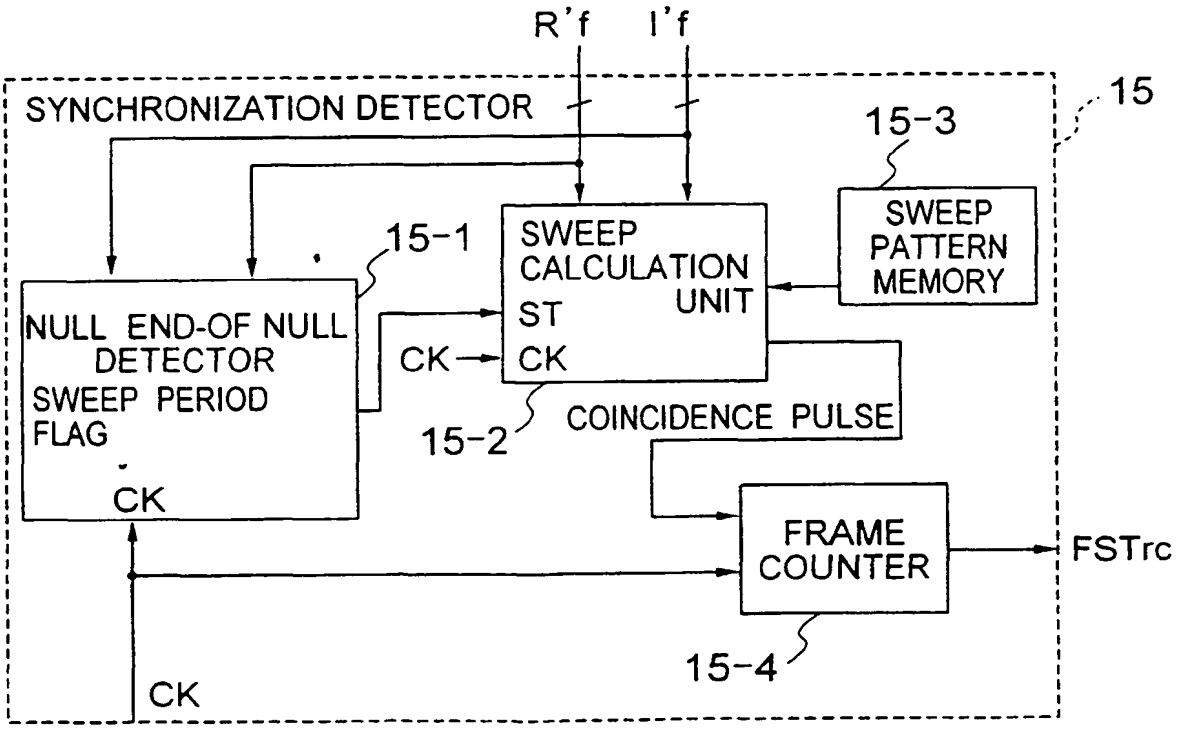

R'f
I'f
SYNCHRONIZATION DETECTOR
15
15-3
SWEEP PATTERN MEMORY
15-1
SWEEP CALCULATION UNIT
ST
CK
NULL END-OF NULL DETECTOR
SWEEP PERIOD FLAG
CK
CK
15-2
COINCIDENCE PULSE
FRAME COUNTER
FSTrc
15-4
CK

FIG. 22

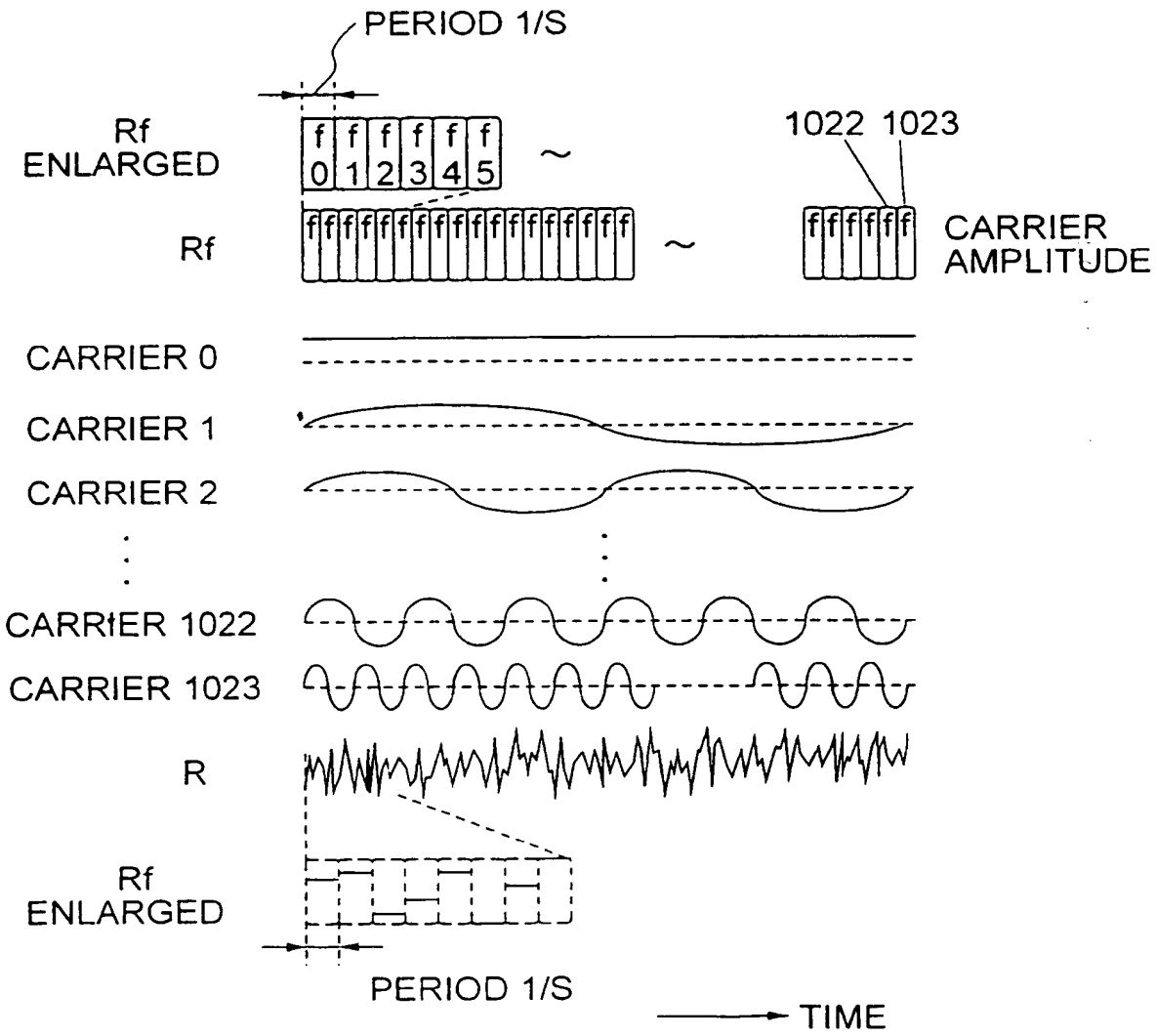

PERIOD 1/S
Rf ENLARGED
f0 f1 f2 f3 f4 f5
1022 1023
Rf
CARRIER AMPLITUDE
CARRIER 0
CARRIER 1
CARRIER 2
CARRIER 1022
CARRIER 1023
R
Rf ENLARGED
PERIOD 1/S
TIME

FIG. 23 A

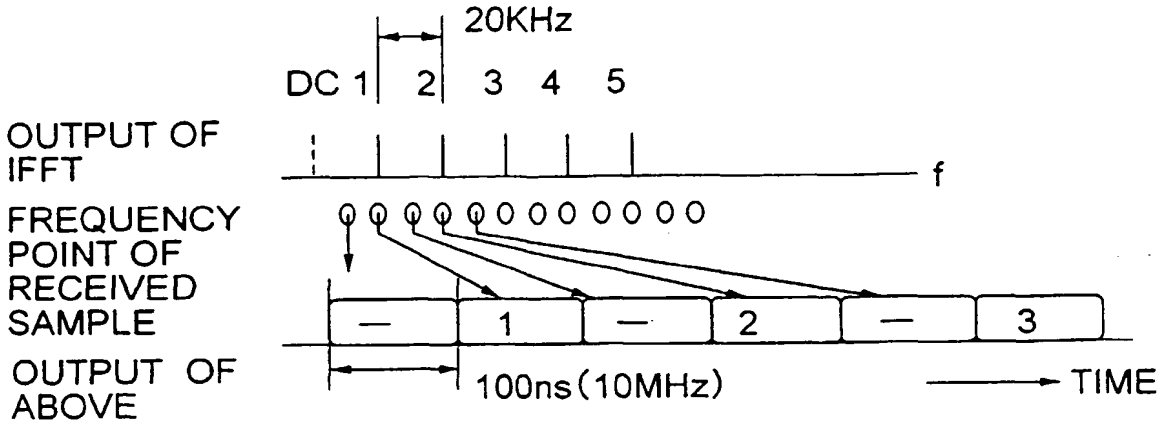


FIG. 23 B

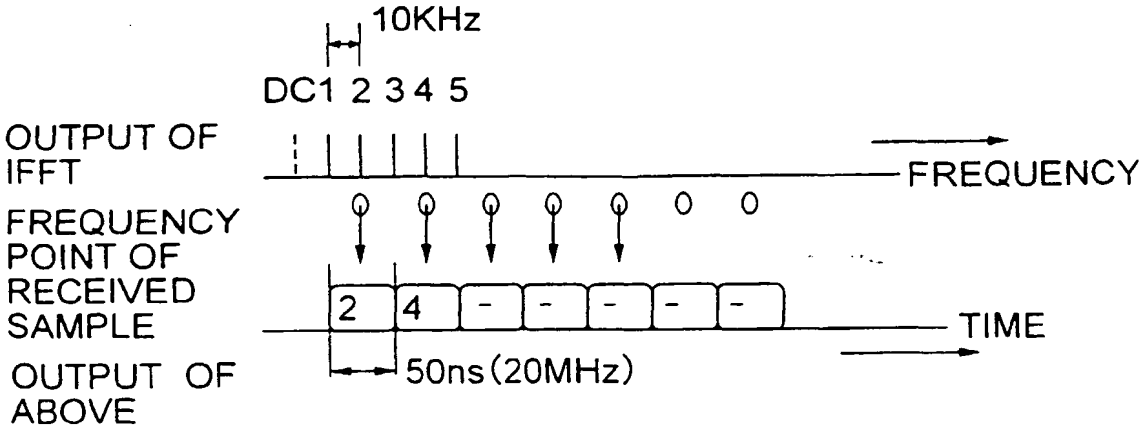


FIG. 23C

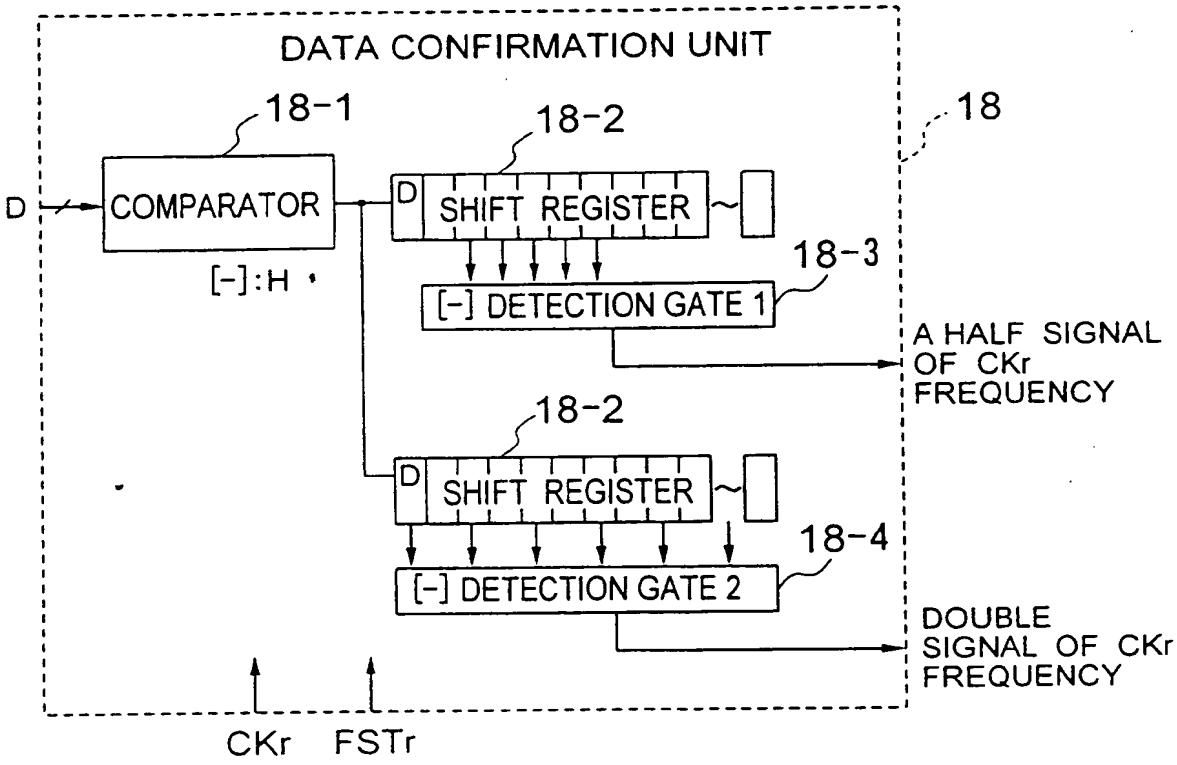

DATA CONFIRMATION UNIT
18
18-1
18-2
D
COMPARATOR
[-]:H
SHIFT REGISTER
18-3
[-] DETECTION GATE 1
A HALF SIGNAL OF CKr FREQUENCY
18-2
SHIFT REGISTER
18-4
[-] DETECTION GATE 2
DOUBLE SIGNAL OF CKr FREQUENCY
CKr
FSTr

FIG. 24

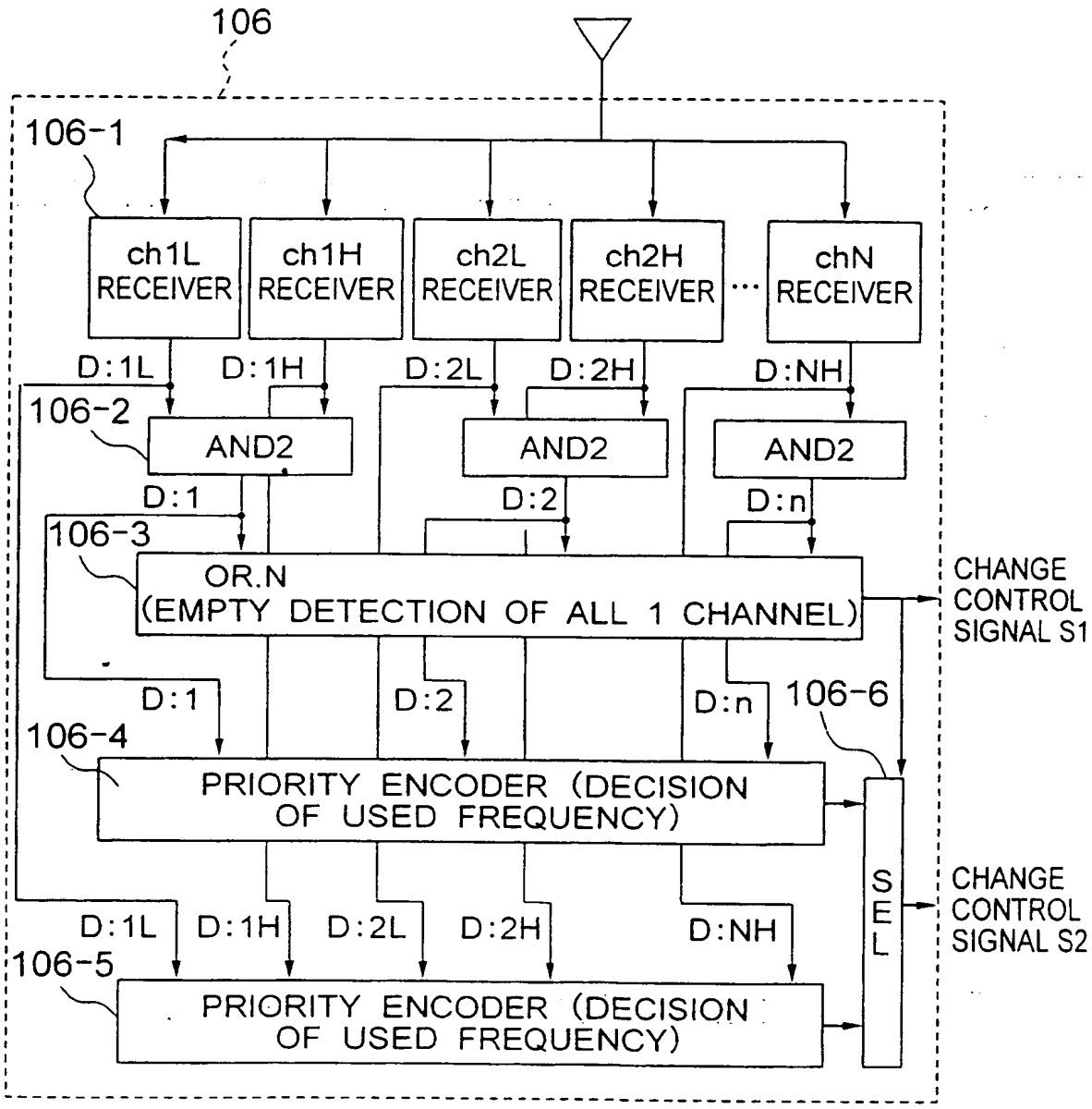

106
106-1
ch1L RECEIVER
ch1H RECEIVER
ch2L RECEIVER
ch2H RECEIVER
chN RECEIVER
D:1L
D:1H
D:2L
D:2H
D:NH
106-2
AND2
AND2
AND2
D:1
D:2
D:n
106-3
OR.N
(EMPTY DETECTION OF ALL 1 CHANNEL)
CHANGE CONTROL SIGNAL S1
D:1
D:2
D:n
106-6
106-4
PRIORITY ENCODER (DECISION OF USED FREQUENCY)
SEL
CHANGE CONTROL SIGNAL S2
D:1L
D:1H
D:2L
D:2H
D:NH
106-5
PRIORITY ENCODER (DECISION OF USED FREQUENCY)

FIG. 25

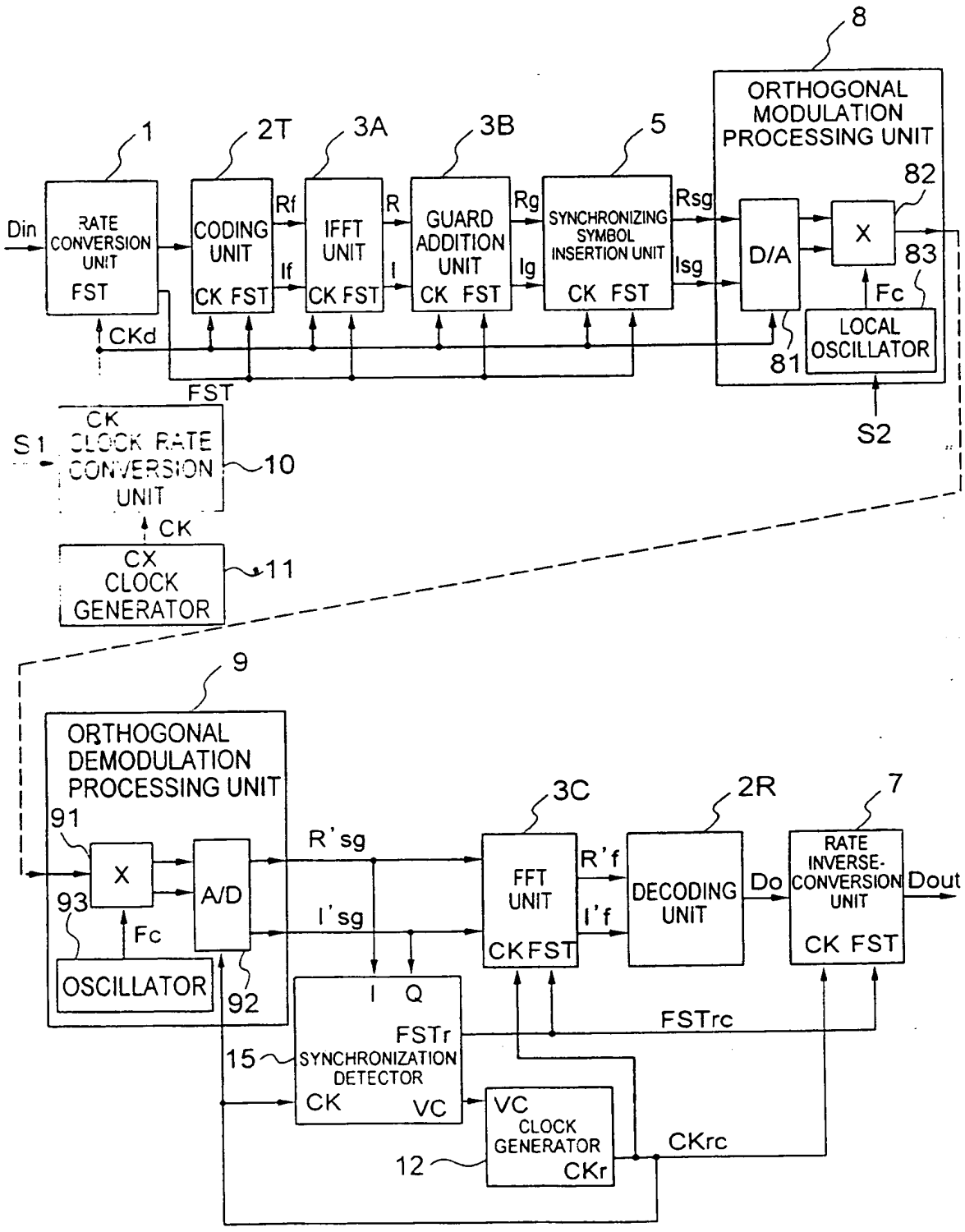

8
ORTHOGONAL MODULATION PROCESSING UNIT
1
2T
3A
3B
5
Din
RATE CONVERSION UNIT
FST
CODING UNIT
CK FST
Rf
If
IFFT UNIT
CK FST
R
I
GUARD ADDITION UNIT
CK FST
Rg
Ig
SYNCHRONIZING SYMBOL INSERTION UNIT
CK FST
Rsg
Isg
D/A
X
82
83
Fc
LOCAL OSCILLATOR
81
CKd
FST
S2
S1
CK CLOCK RATE CONVERSION UNIT
10
CK
CX CLOCK GENERATOR
11
9
ORTHOGONAL DEMODULATION PROCESSING UNIT
91
X
93
Fc
OSCILLATOR
A/D
92
R'sg
I'sg
3C
FFT UNIT
CKFST
R'f
I'f
2R
DECODING UNIT
Do
7
RATE INVERSE-CONVERSION UNIT
CK FST
Dout
I Q
FSTr
15
SYNCHRONIZATION DETECTOR
CK
VC
FSTrc
VC CLOCK GENERATOR
CKr
12
CKrc

FIG. 26 A

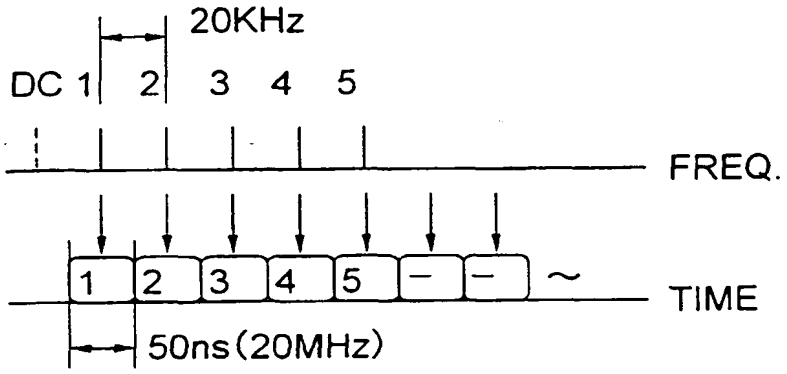


FIG. 26 B

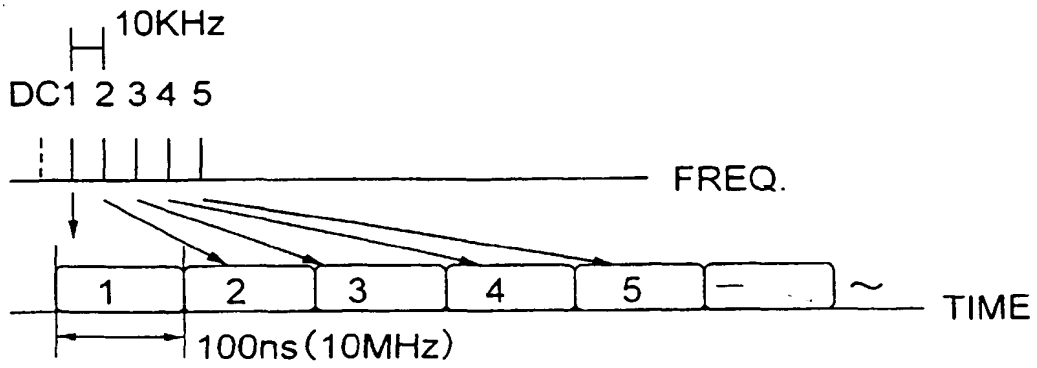


FIG. 27

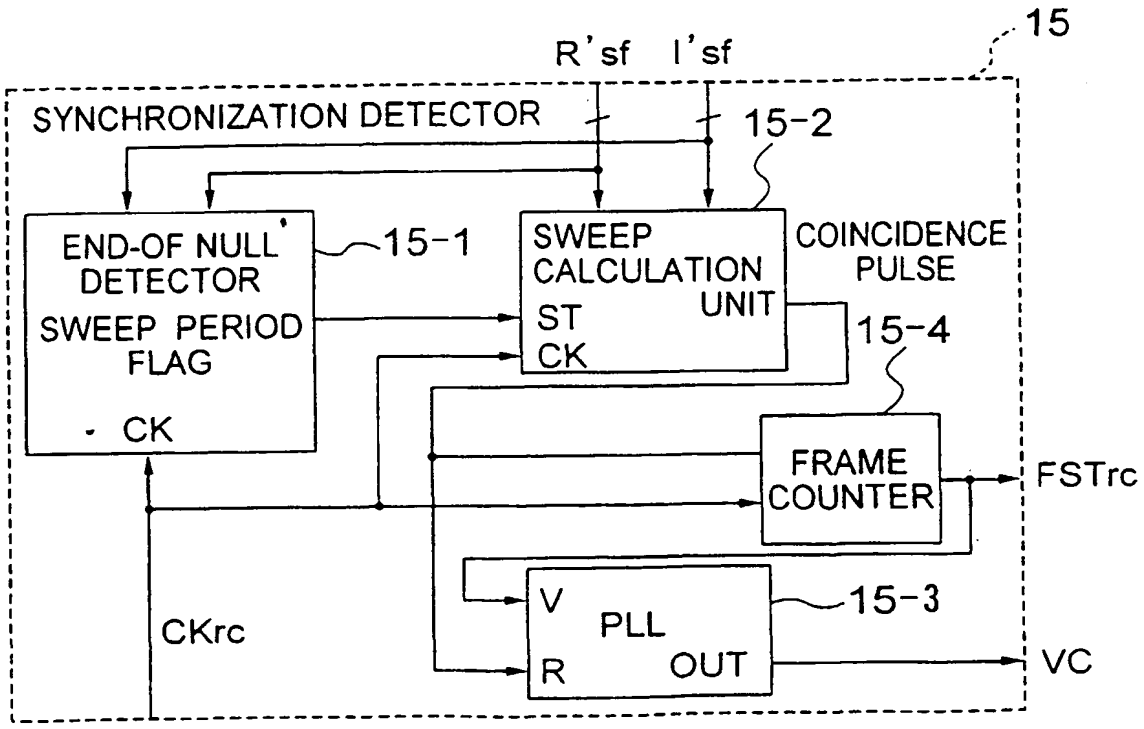

15
R'sf I'sf
SYNCHRONIZATION DETECTOR
15-2
END-OF NULL DETECTOR
SWEEP PERIOD FLAG
CK
15-1
SWEEP CALCULATION UNIT
ST
CK
COINCIDENCE PULSE
15-4
FRAME COUNTER
FSTrc
V
PLL
R
OUT
15-3
VC
CKrc

FIG. 28

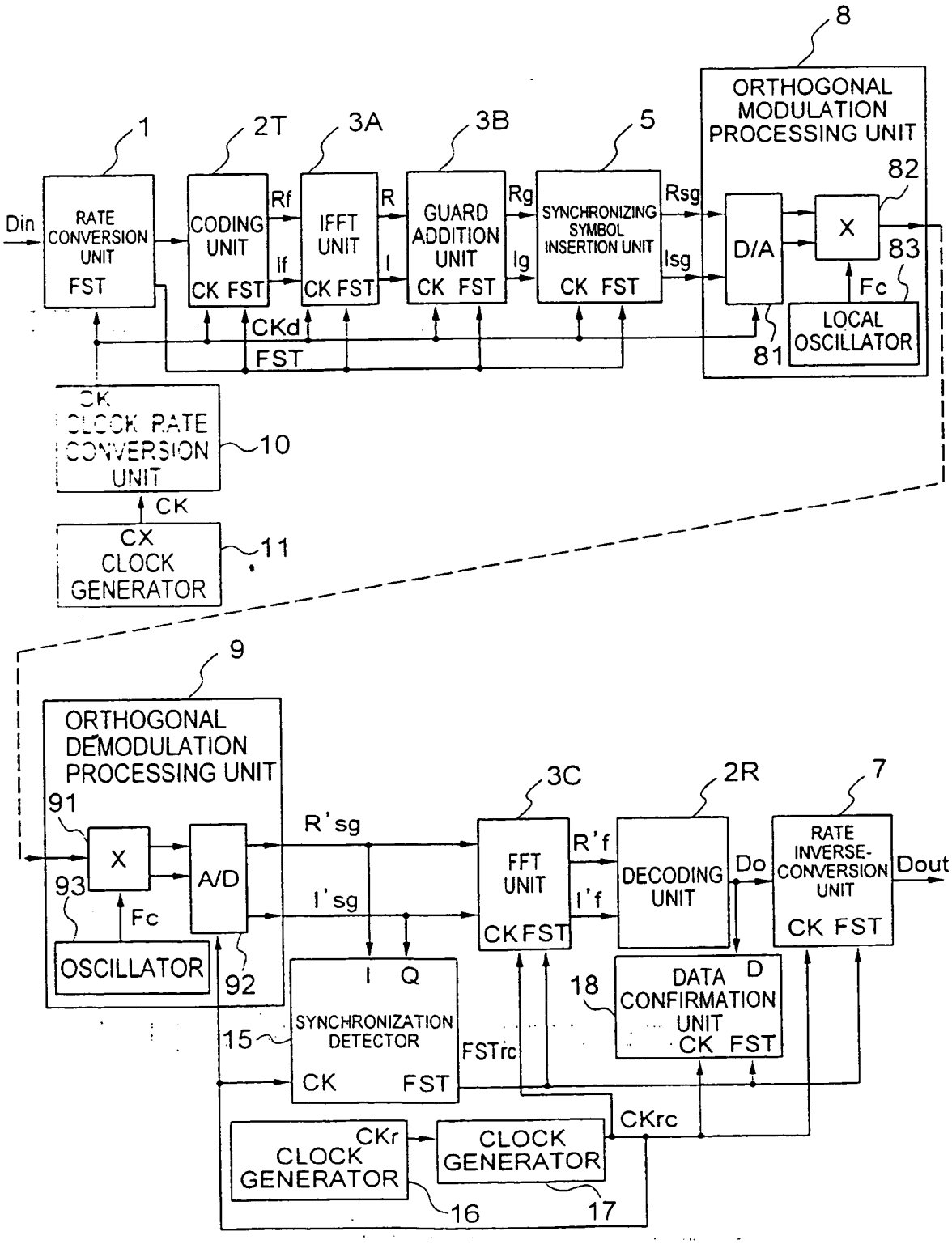

8
ORTHOGONAL MODULATION PROCESSING UNIT
1
2T
3A
3B
5
Din
RATE CONVERSION UNIT
FST
CODING UNIT
CK FST
Rf
If
IFFT UNIT
CK FST
R
I
GUARD ADDITION UNIT
CK FST
Rg
Ig
SYNCHRONIZING SYMBOL INSERTION UNIT
CK FST
Rsg
Isg
D/A
X
82
83
Fc
LOCAL OSCILLATOR
81
CKd
FST
CK CLOCK RATE CONVERSION UNIT
10
CK
CX CLOCK GENERATOR
11
9
ORTHOGONAL DEMODULATION PROCESSING UNIT
91
X
93
Fc
OSCILLATOR
A/D
92
R'sg
I'sg
3C
FFT UNIT
CKFST
R'f
I'f
2R
DECODING UNIT
Do
7
RATE INVERSE-CONVERSION UNIT
CK FST
Dout
I Q
SYNCHRONIZATION DETECTOR
15
CK FST
FSTrc
18
DATA CONFIRMATION UNIT
D
CK FST
CKrc
CKr
CLOCK GENERATOR
16
CLOCK GENERATOR
17

FIG. 29

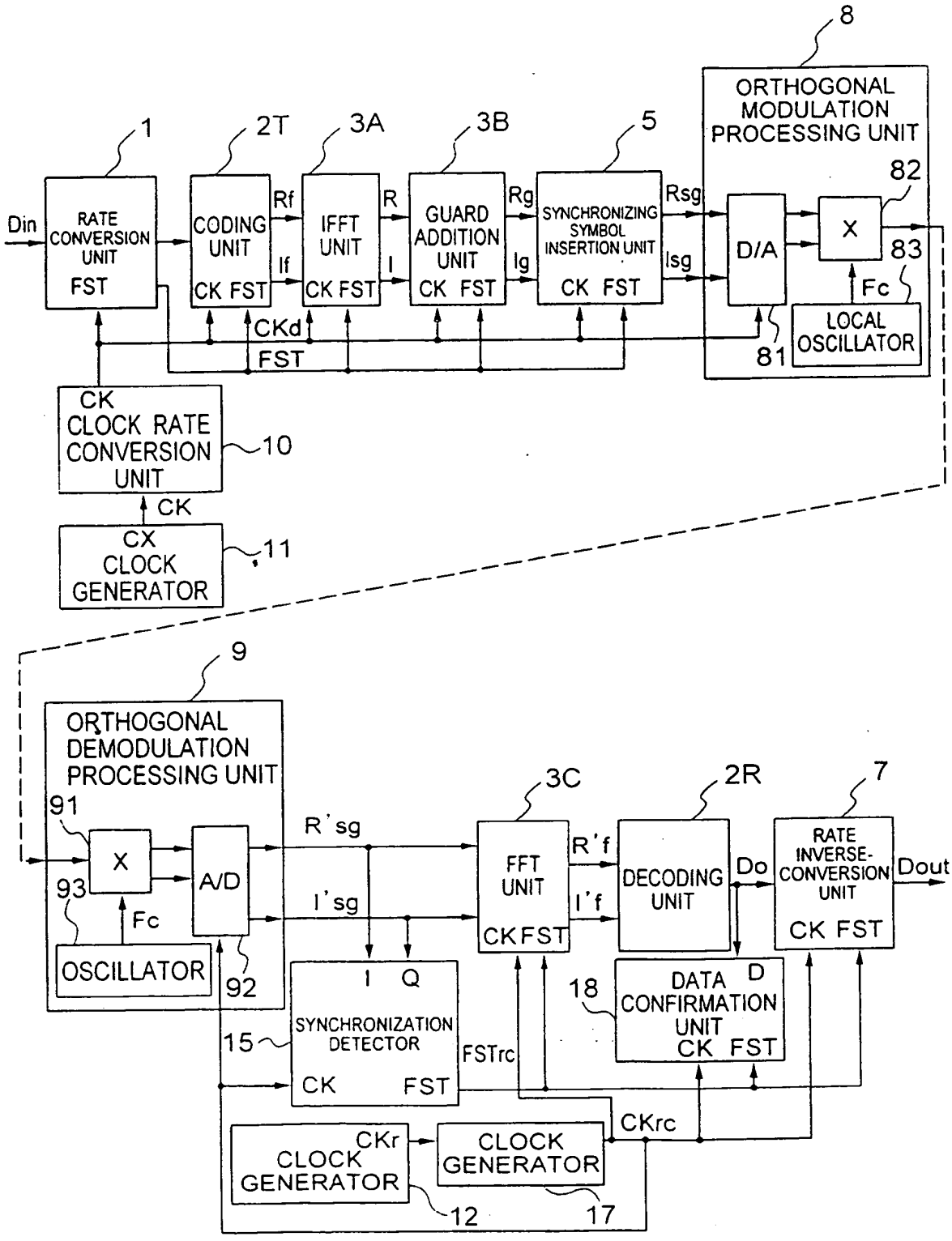

8
ORTHOGONAL MODULATION PROCESSING UNIT
1
2T
3A
3B
5
Din
RATE CONVERSION UNIT
FST
CODING UNIT
CK FST
Rf
If
IFFT UNIT
CK FST
R
I
GUARD ADDITION UNIT
CK FST
Rg
Ig
SYNCHRONIZING SYMBOL INSERTION UNIT
CK FST
Rsg
Isg
D/A
X
82
83
Fc
LOCAL OSCILLATOR
81
CKd
FST
CK CLOCK RATE CONVERSION UNIT
10
CK
CX CLOCK GENERATOR
11
9
ORTHOGONAL DEMODULATION PROCESSING UNIT
91
X
93
Fc
OSCILLATOR
A/D
92
R'sg
I'sg
3C
FFT UNIT
CKFST
R'f
I'f
2R
DECODING UNIT
Do
7
RATE INVERSE-CONVERSION UNIT
CK FST
Dout
I Q
SYNCHRONIZATION DETECTOR
15
CK FST
FSTrc
18
DATA CONFIRMATION UNIT
D
CK FST
CKrc
CKr
CLOCK GENERATOR
12
CLOCK GENERATOR
17

FIG. 30

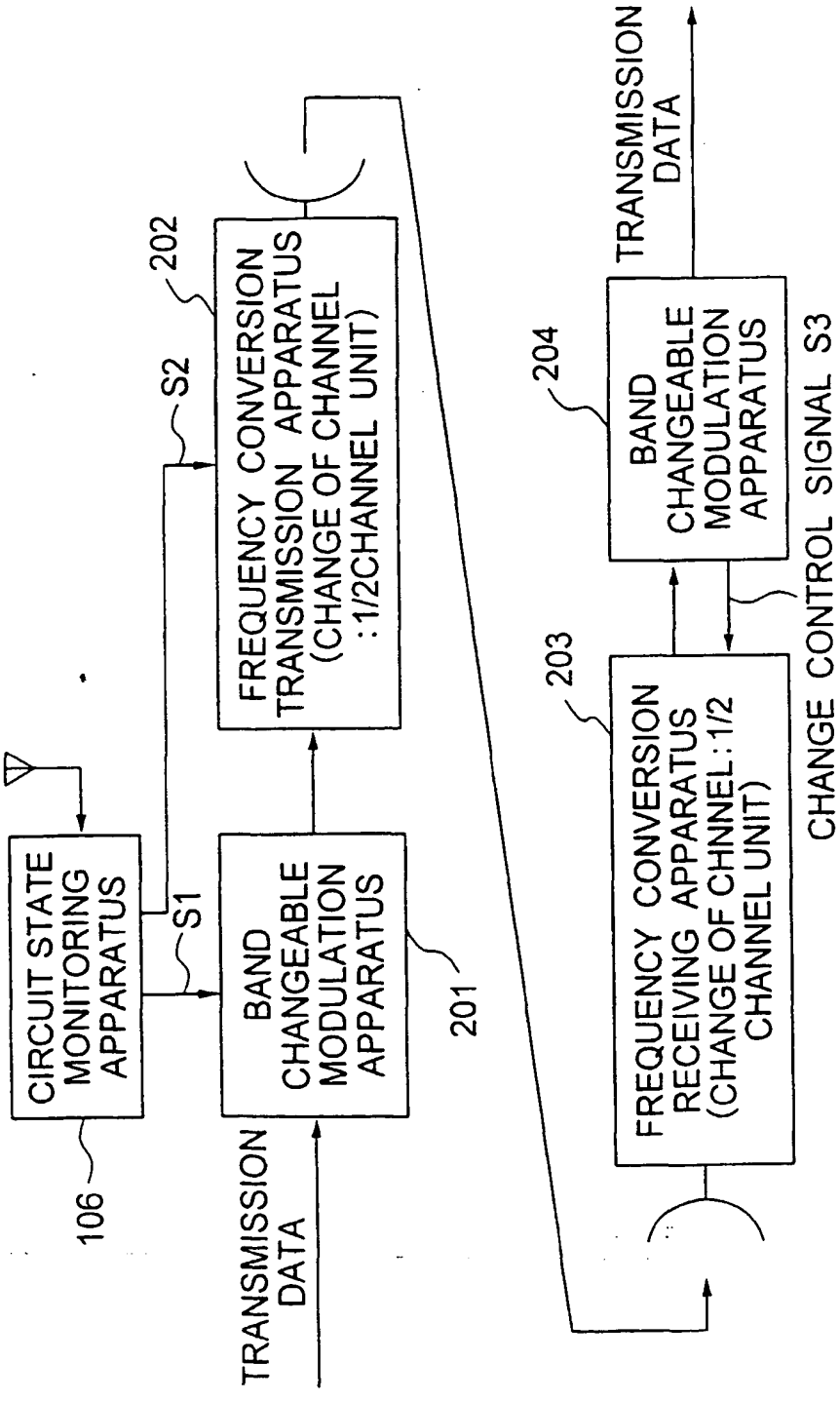

CIRCUIT STATE MONITORING APPARATUS
106
S1
S2
BAND CHANGEABLE MODULATION APPARATUS
201
TRANSMISSION DATA
FREQUENCY CONVERSION TRANSMISSION APPARATUS (CHANGE OF CHANNEL : 1/2CHANNEL UNIT)
202
FREQUENCY CONVERSION RECEIVING APPARATUS (CHANGE OF CHNNEL : 1/2 CHANNEL UNIT)
203
BAND CHANGEABLE MODULATION APPARATUS
204
TRANSMISSION DATA
CHANGE CONTROL SIGNAL S3

FIG. 31

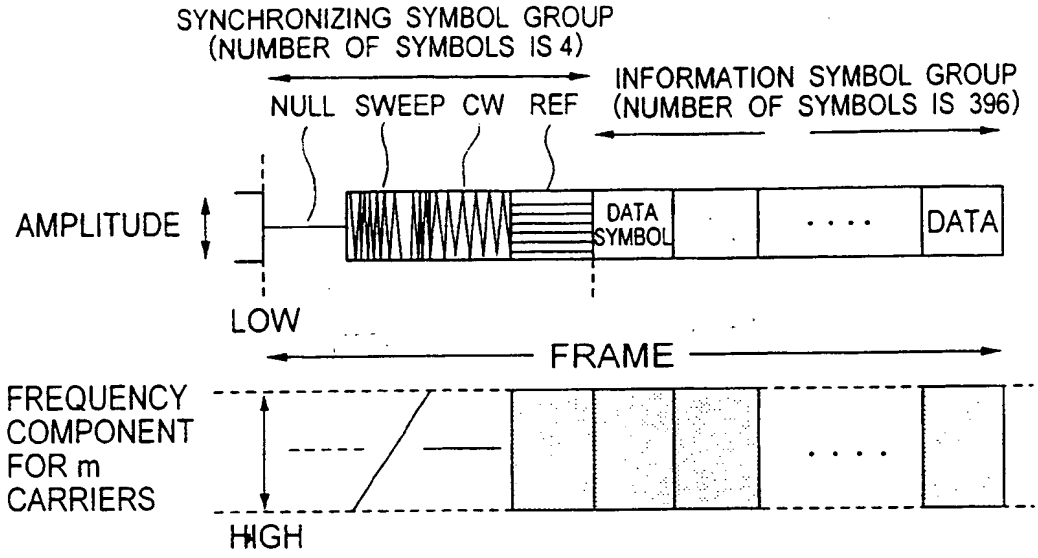
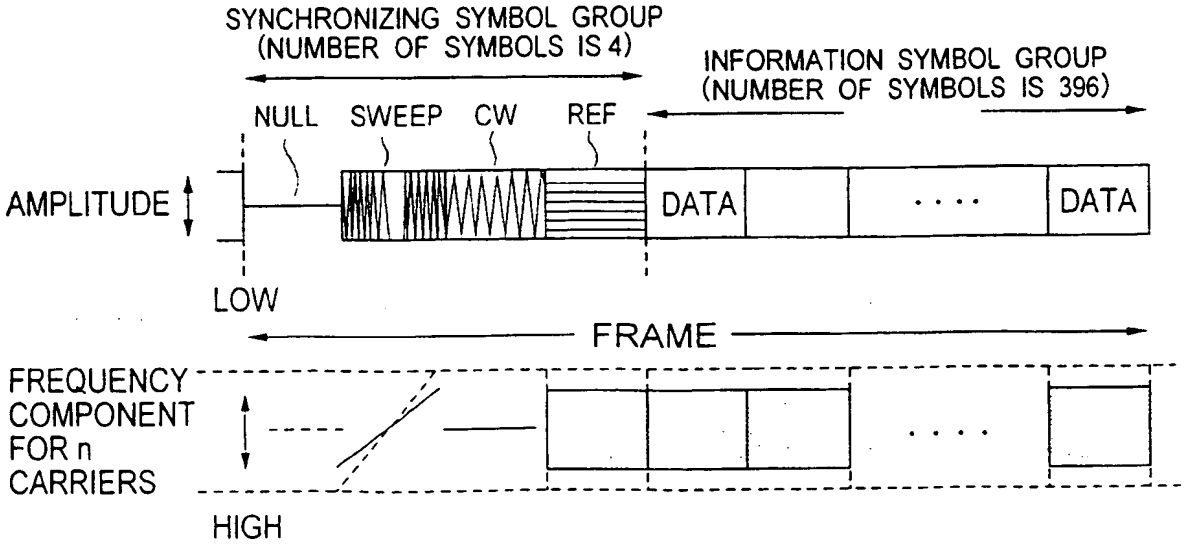

SYNCHRONIZING SYMBOL GROUP
(NUMBER OF SYMBOLS IS 4)
INFORMATION SYMBOL GROUP
(NUMBER OF SYMBOLS IS 396)
NULL
SWEEP
CW
REF
DATA SYMBOL
DATA
AMPLITUDE
LOW
FRAME
FREQUENCY COMPONENT FOR m CARRIERS
HIGH

FIG. 32


SYNCHRONIZING SYMBOL GROUP
(NUMBER OF SYMBOLS IS 4)
INFORMATION SYMBOL GROUP
(NUMBER OF SYMBOLS IS 396)
NULL
SWEEP
CW
REF
DATA
DATA
AMPLITUDE
LOW
FRAME
FREQUENCY COMPONENT FOR n CARRIERS
HIGH

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